



Q67H2-AD

Rev : 1.0

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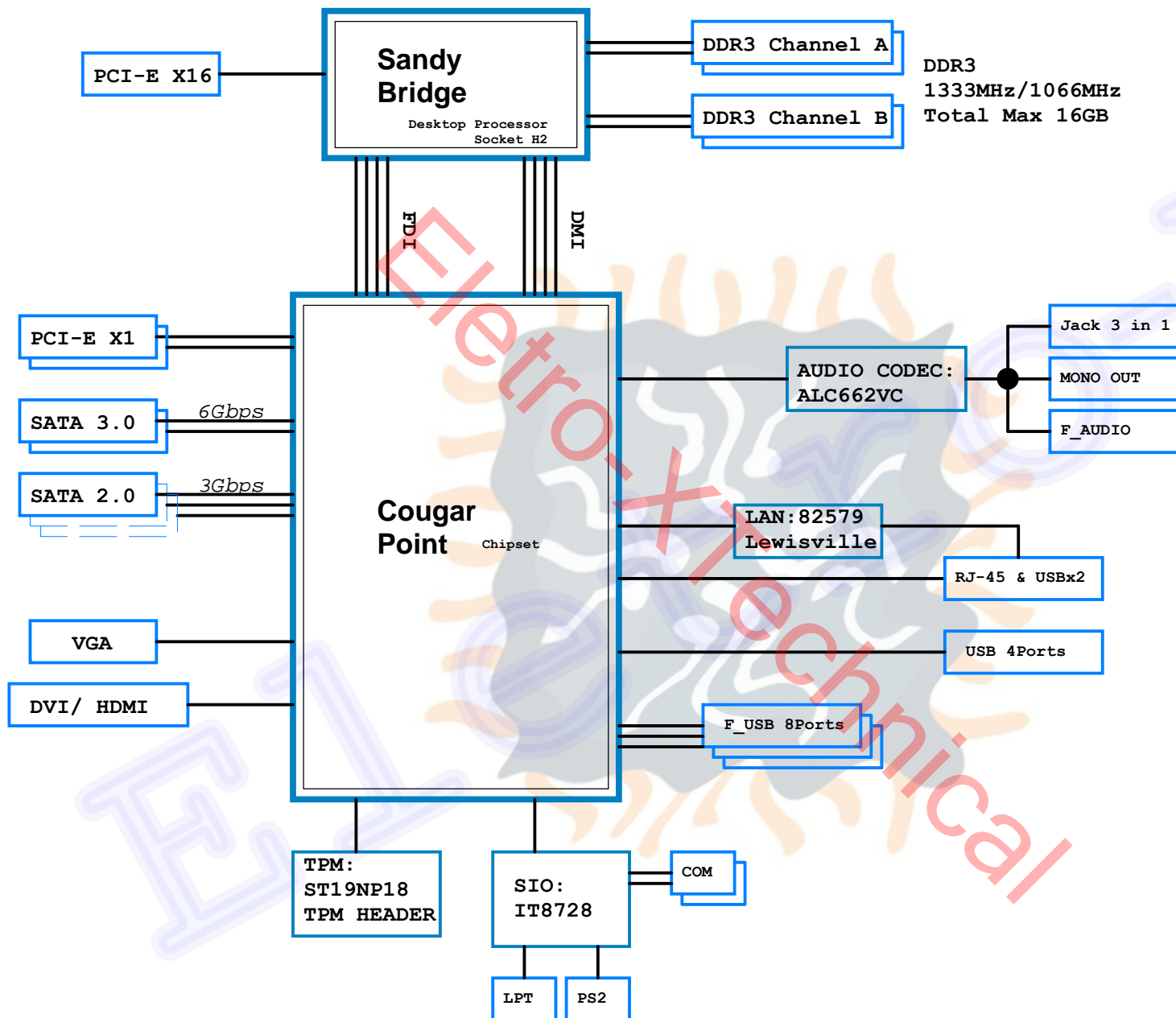
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NOTE:

REVISION HISTORY:

Rev	Date	Notes
V.A	2010/07/22	Initial version
V.B	2010/08/24	
V.C	2010/09/10	
V.1.0	2010/09/16	

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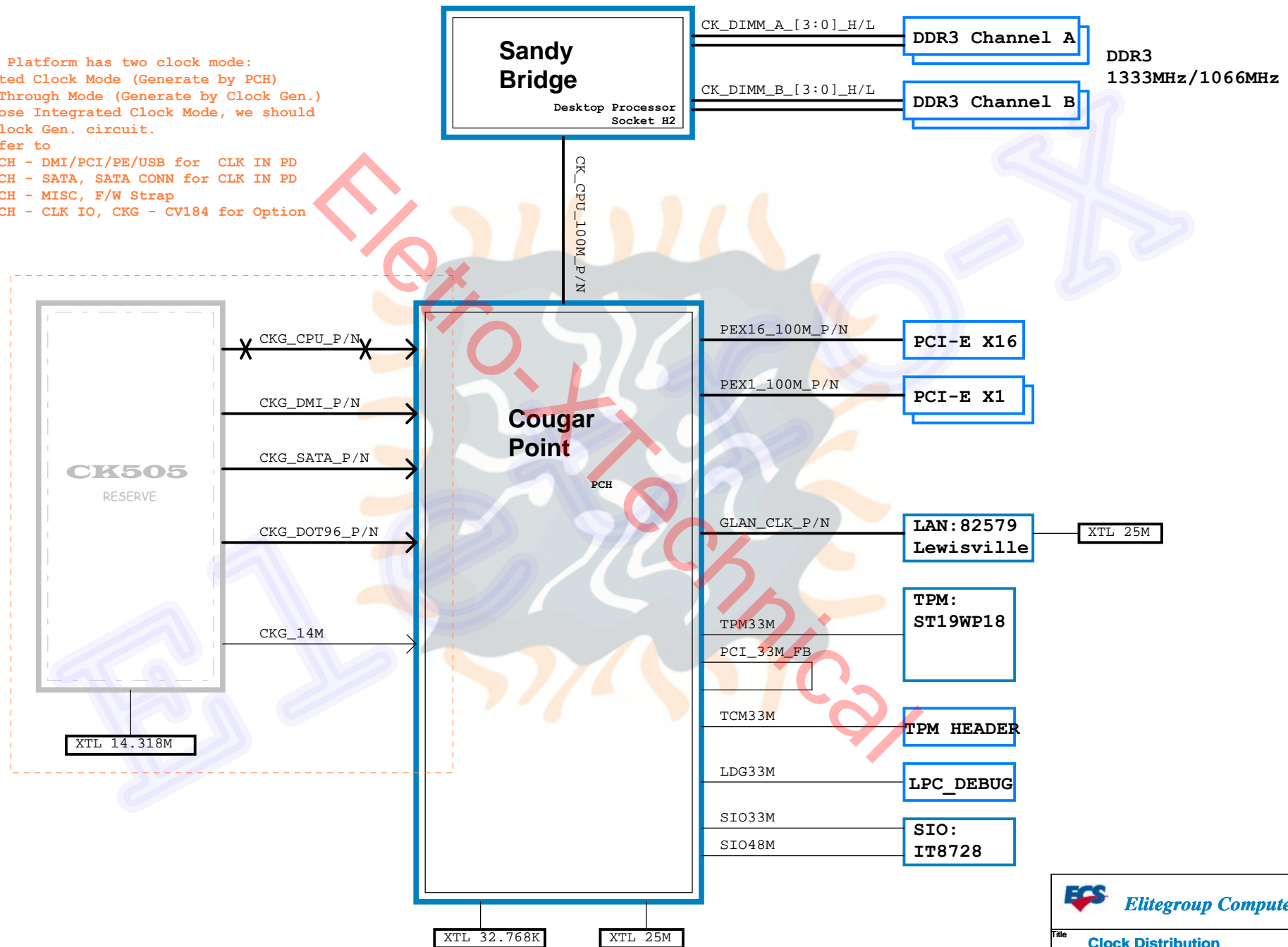
Sugar Bay Platform has two clock mode:

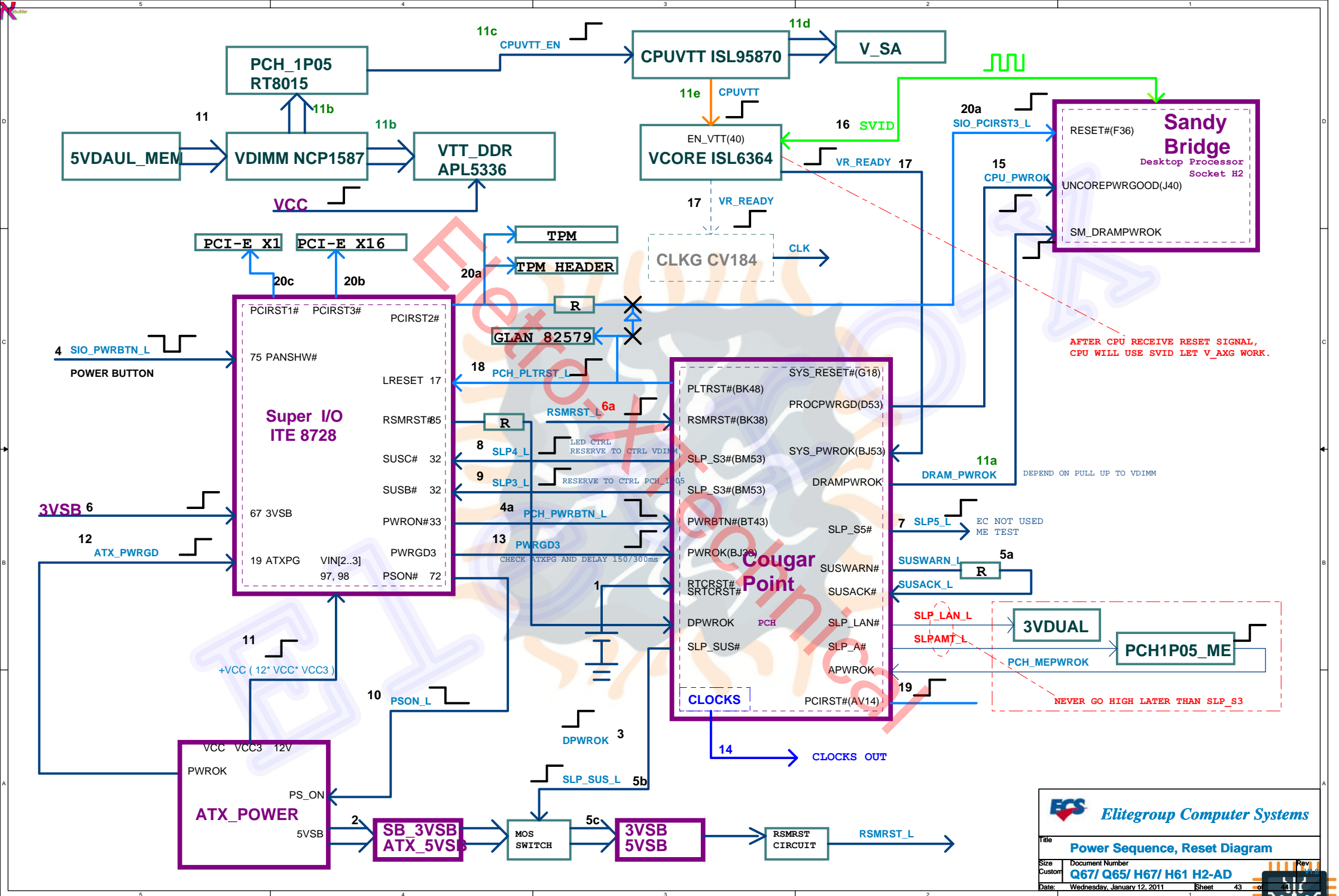
1. Integrated Clock Mode (Generate by PCH)
2. Buffer Through Mode (Generate by Clock Gen.)

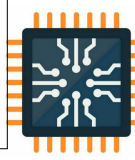
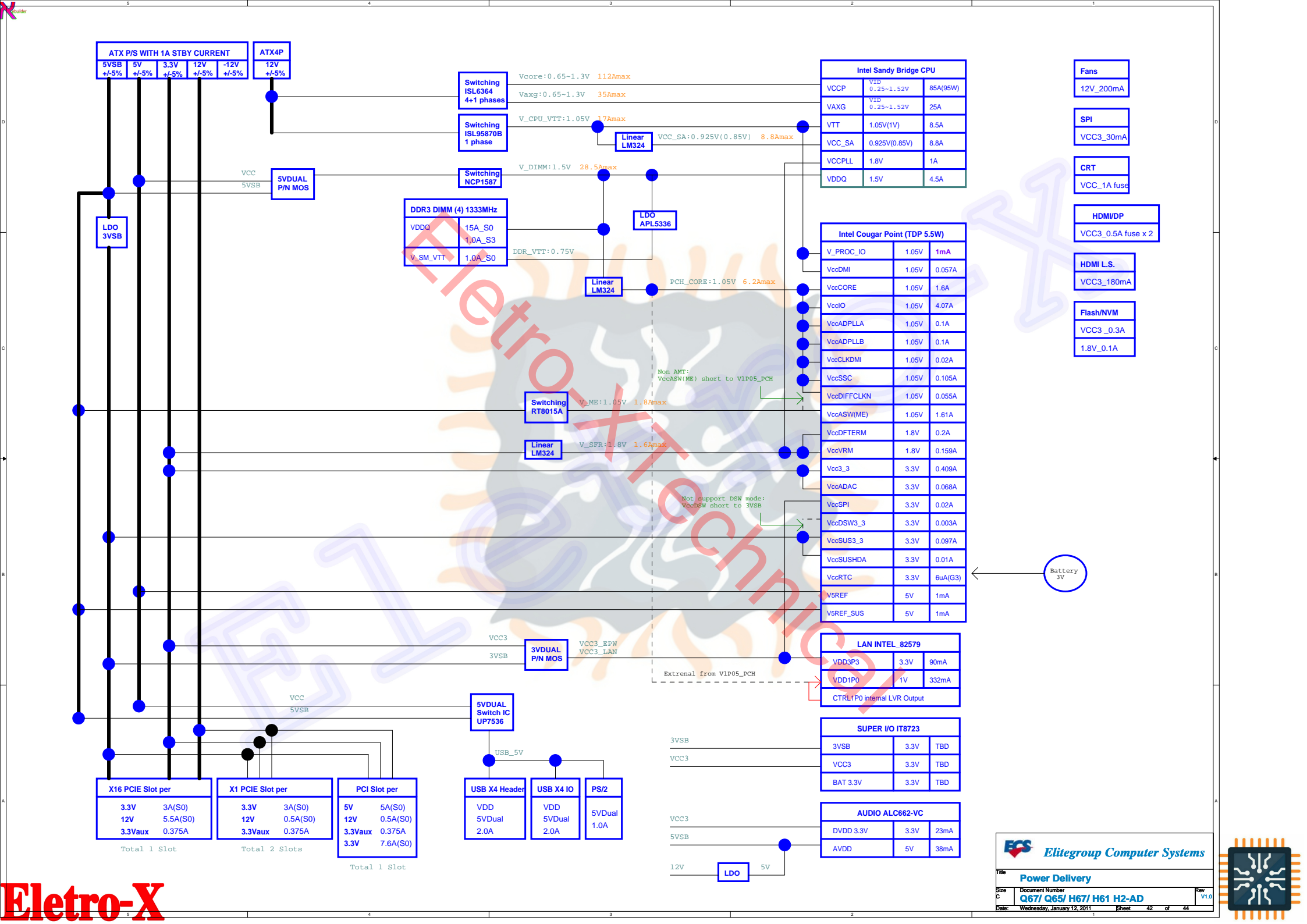
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

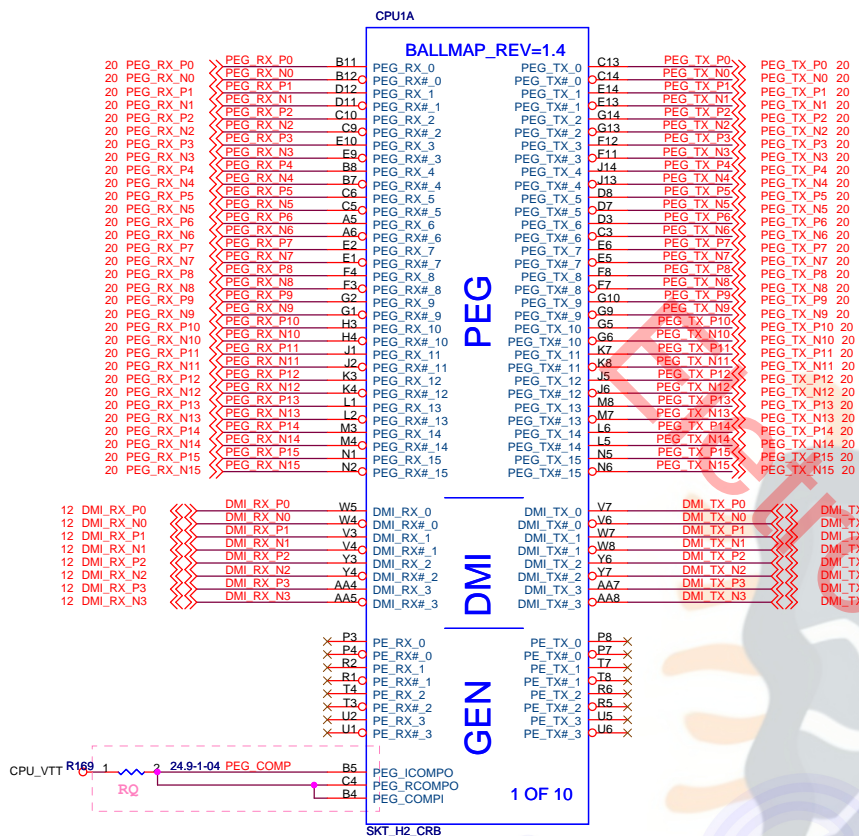
Please refer to

- Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
- Page.13 PCH - SATA, SATA CONN for CLK IN PD
- Page.14 PCH - MISC, F/W Strap
- Page.15 PCH - CLK IO, CKG - CV184 for Option

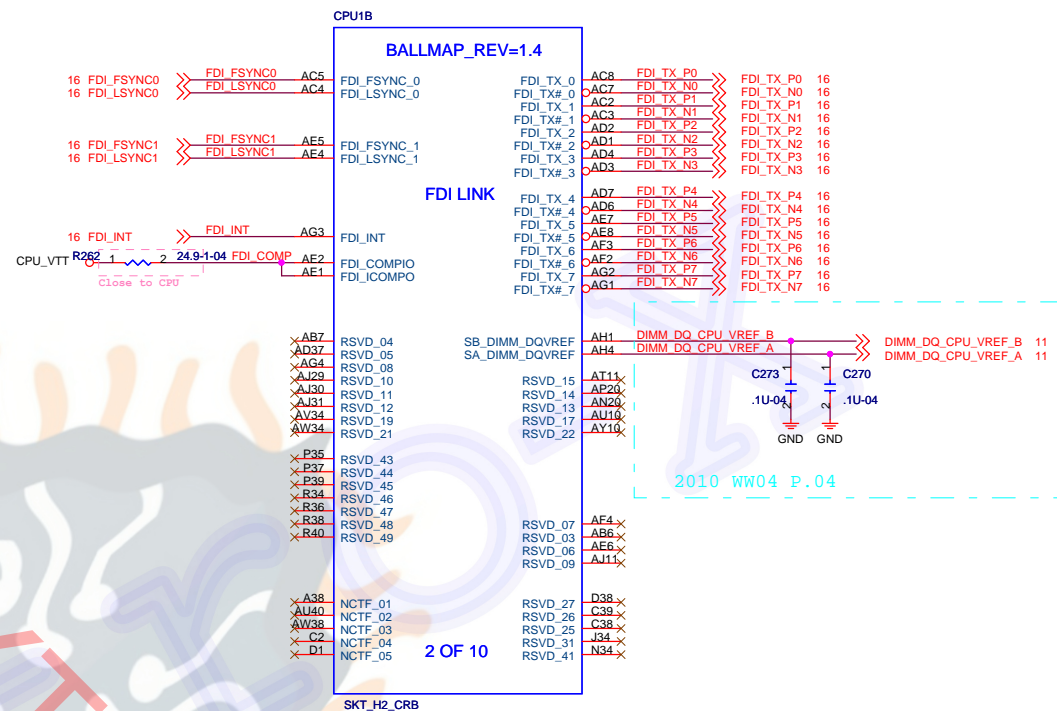








SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ. 1
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.



9 M_DATA_A[0..63]	← M_DATA A[0..63]
9 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
9 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
9 M_MA_A[0..15]	← M_MA A[0..15]
9 M_BS_A[0..2]	← M_BS A[0..2]
9 M_CS_A_L[0..3]	← M_CS A L[0..3]
9 M_CKE_A[0..3]	← M_CKE A[0..3]
9 M_ODT_A[0..3]	← M_ODT A[0..3]
9 M_CLK_A_P[0..3]	← M_CLK A P[0..3]
9 M_CLK_A_N[0..3]	← M_CLK A N[0..3]

DDR3 CH.A

9,10 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

10 M_DATA_B[0..63]	← M_DATA B[0..63]
10 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
10 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
10 M_MA_B[0..15]	← M_MA B[0..15]
10 M_BS_B[0..2]	← M_BS B[0..2]
10 M_CS_B_L[0..3]	← M_CS B L[0..3]
10 M_CKE_B[0..3]	← M_CKE B[0..3]
10 M_ODT_B[0..3]	← M_ODT B[0..3]
10 M_CLK_B_P[0..3]	← M_CLK B P[0..3]
10 M_CLK_B_N[0..3]	← M_CLK B N[0..3]

DDR3 CH.B

10 M_WE_B_L	← M_WE B_L
10 M_CAS_B_L	← M_CAS B_L
10 M_RAS_B_L	← M_RAS B_L

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_MA_4
M_DATA_A5	AL1	SA_DQ_5
M_DATA_A6	AL2	SA_DQ_6
M_DATA_A7	AN1	SA_DQ_7
M_DATA_A8	AN4	SA_DQ_8
M_DATA_A9	AR3	SA_DQ_9
M_DATA_A10	AR4	SA_DQ_10
M_DATA_A11	AN2	SA_DQ_11
M_DATA_A12	AR2	SA_DQ_12
M_DATA_A13	AR1	SA_DQ_13
M_DATA_A14	AR2	SA_DQ_14
M_DATA_A15	AR1	SA_DQ_15
M_DATA_A16	AV2	SA_DQ_16
M_DATA_A17	AW3	SA_DQ_17
M_DATA_A18	AV5	SA_DQ_18
M_DATA_A19	AU2	SA_DQ_19
M_DATA_A20	AU3	SA_DQ_20
M_DATA_A21	AU3	SA_DQ_21
M_DATA_A22	AU5	SA_DQ_22
M_DATA_A23	AV5	SA_DQ_23
M_DATA_A24	AV7	SA_DQ_24
M_DATA_A25	AU7	SA_DQ_25
M_DATA_A26	AV9	SA_DQ_26
M_DATA_A27	AU9	SA_DQ_27
M_DATA_A28	AV7	SA_DQ_28
M_DATA_A29	AW7	SA_DQ_29
M_DATA_A30	AW5	SA_DQ_30
M_DATA_A31	AY9	SA_DQ_31
M_DATA_A32	AU35	SA_DQ_32
M_DATA_A33	AW37	SA_DQ_33
M_DATA_A34	AU39	SA_DQ_34
M_DATA_A35	AW35	SA_DQ_35
M_DATA_A36	AY36	SA_DQ_36
M_DATA_A37	AU38	SA_DQ_37
M_DATA_A38	AU37	SA_DQ_38
M_DATA_A39	AR37	SA_DQ_39
M_DATA_A40	AR37	SA_DQ_40
M_DATA_A41	AN36	SA_DQ_41
M_DATA_A42	AN37	SA_DQ_42
M_DATA_A43	AR39	SA_DQ_43
M_DATA_A44	AR38	SA_DQ_44
M_DATA_A45	AN38	SA_DQ_45
M_DATA_A46	AN40	SA_DQ_46
M_DATA_A47	AL40	SA_DQ_47
M_DATA_A48	AL37	SA_DQ_48
M_DATA_A49	AJ38	SA_DQ_49
M_DATA_A50	AJ37	SA_DQ_50
M_DATA_A51	AL38	SA_DQ_51
M_DATA_A52	AL38	SA_DQ_52
M_DATA_A53	AJ39	SA_DQ_53
M_DATA_A54	AJ40	SA_DQ_54
M_DATA_A55	AG40	SA_DQ_55
M_DATA_A56	AG37	SA_DQ_56
M_DATA_A57	AE38	SA_DQ_57
M_DATA_A58	AE37	SA_DQ_58
M_DATA_A59	AG39	SA_DQ_59
M_DATA_A60	AG38	SA_DQ_60
M_DATA_A61	AE39	SA_DQ_61
M_DATA_A62	AE40	SA_DQ_62
M_DATA_A63	AE40	SA_DQ_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7

M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW8	SA_DQS#_3
M_DQS_A_N4	AV36	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

SM_DRAMRST#

SA_DQS_8
SA_DQS#_8

SA_ECC_CB_0
SA_ECC_CB_1
SA_ECC_CB_2
SA_ECC_CB_3
SA_ECC_CB_4
SA_ECC_CB_5
SA_ECC_CB_6
SA_ECC_CB_7

DDR_0

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SKT_H2_CRB

DDR3 CH.A

BALLMAP_REV=1.4

SA_MA_0	AV27	M_MA_A0
SA_MA_1	AV24	M_MA_A1
SA_MA_2	AW24	M_MA_A2
SA_MA_3	AW23	M_MA_A3
SA_MA_4	AV23	M_MA_A4
SA_MA_5	AT24	M_MA_A5
SA_MA_6	AT23	M_MA_A6
SA_MA_7	AJ22	M_MA_A7
SA_MA_8	AV22	M_MA_A8
SA_MA_9	AT22	M_MA_A9
SA_MA_10	AV28	M_MA_A10
SA_MA_11	AJ21	M_MA_A11
SA_MA_12	AT21	M_MA_A12
SA_MA_13	AW22	M_MA_A13
SA_MA_14	AJ20	M_MA_A14
SA_MA_15	AT20	M_MA_A15

SA_WE#	AW29	M_WE_A_L
SA_CAS#	AW30	M_CAS_A_L
SA_RAS#	AJ28	M_RAS_A_L

SA_BS_0	AY29	M_BS_A0
SA_BS_1	AW28	M_BS_A1
SA_BS_2	AV20	M_BS_A2

SA_CS#_0	AU29	M_CS_A_L0
SA_CS#_1	AW30	M_CS_A_L1
SA_CS#_2	AW30	M_CS_A_L2
SA_CS#_3	AJ33	M_CS_A_L3

SA_CKE_0	AV19	M_CKE_A0
SA_CKE_1	AT19	M_CKE_A1
SA_CKE_2	AV18	M_CKE_A2
SA_CKE_3	AV18	M_CKE_A3

SA_ODT_0	AY31	M_ODT_A0
SA_ODT_1	AJ32	M_ODT_A1
SA_ODT_2	AJ30	M_ODT_A2
SA_ODT_3	AW33	M_ODT_A3

SA_CK_0	AY25	M_CLK_A_P0
SA_CK#_0	AW25	M_CLK_A_N0
SA_CK_1	AJ24	M_CLK_A_P1
SA_CK#_1	AJ25	M_CLK_A_N1
SA_CK_2	AY27	M_CLK_A_P2
SA_CK#_2	AV26	M_CLK_A_P3
SA_CK_3	AW26	M_CLK_A_N3

SM_DRAMRST#

SA_DQS_8
SA_DQS#_8

SA_ECC_CB_0
SA_ECC_CB_1
SA_ECC_CB_2
SA_ECC_CB_3
SA_ECC_CB_4
SA_ECC_CB_5
SA_ECC_CB_6
SA_ECC_CB_7

DDR_0

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SKT_H2_CRB

DDR3 CH.A

Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ8	SB_DQ_2
M_DATA_B3	AG5	SB_DQ_3
M_DATA_B4	AG6	SB_DQ_4
M_DATA_B5	AJ6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AL7	SB_DQ_7
M_DATA_B8	AM7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B10	AM10	SB_DQ_10
M_DATA_B11	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B13	AL9	SB_DQ_13
M_DATA_B14	AM9	SB_DQ_14
M_DATA_B15	AP7	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AR7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AR9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL13	SB_DQ_29
M_DATA_B30	AP12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR35	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B49	AM31	SB_DQ_49
M_DATA_B50	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B52	AM34	SB_DQ_52
M_DATA_B53	AL31	SB_DQ_53
M_DATA_B54	AM35	SB_DQ_54
M_DATA_B55	AL34	SB_DQ_55
M_DATA_B56	AH35	SB_DQ_56
M_DATA_B57	AH34	SB_DQ_57
M_DATA_B58	AE34	SB_DQ_58
M_DATA_B59	AE35	SB_DQ_59
M_DATA_B60	AJ35	SB_DQ_60
M_DATA_B61	AJ34	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN3	SB_DQS_3
M_DQS_B_P4	AN3	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7

M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN28	SB_DQS#_4
M_DQS_B_N5	AR33	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

BALLMAP_REV=1.4

SB_MA_0	AK24	M_MA_B0
SB_MA_1	AM20	M_MA_B1
SB_MA_2	AM19	M_MA_B2
SB_MA_3	AK18	M_MA_B3
SB_MA_4	AP19	M_MA_B4
SB_MA_5	AP18	M_MA_B5
SB_MA_6	AM18	M_MA_B6
SB_MA_7	AL18	M_MA_B7
SB_MA_8	AN18	M_MA_B8
SB_MA_9	AY17	M_MA_B9
SB_MA_10	AN23	M_MA_B10
SB_MA_11	AU17	M_MA_B11
SB_MA_12	AT18	M_MA_B12
SB_MA_13	AR26	M_MA_B13
SB_MA_14	AY16	M_MA_B14
SB_MA_15	AV16	M_MA_B15

SA_CK[2]	AR25	M_WE_B_L
SA_CK[1]	AK25	M_CAS_B_L
SA_ODT[2]	AP24	M_RAS_B_L

SB_BS_0	AP23	M_BS_B0
SB_BS_1	AM24	M_BS_B1
SB_BS_2	AW17	M_BS_B2

SB_CS#_0	AN25	M_CS_B_L0
SB_CS#_1	AN26	M_CS_B_L1
SB_CS#_2	AN25	M_CS_B_L2
SB_CS#_3	AT26	M_CS_B_L3

SB_CKE_0	AU16	M_CKE_B0
SB_CKE_1	AY15	M_CKE_B1
SB_CKE_2	AW15	M_CKE_B2
SB_CKE_3	AV15	M_CKE_B3

SB_ODT_0	AL26	M_ODT_B0
SB_ODT_1	AP26	M_ODT_B1
SB_ODT_2	AM26	M_ODT_B2
SB_ODT_3	AK26	M_ODT_B3

SB_CK_0	AL21	M_CLK_B_P0
SB_CK#_0	AL22	M_CLK_B_N0
SB_CK_1	AL20	M_CLK_B_P1
SB_CK#_1	AK20	M_CLK_B_N1
SB_CK_2	AL23	M_CLK_B_P2
SB_CK#_2	AM22	M_CLK_B_N2
SB_CK_3	AP21	M_CLK_B_P3
SB_CK#_3	AN21	M_CLK_B_N3

SB_DQS_8
SB_DQS#_8

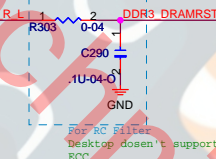
SB_ECC_CB_0
SB_ECC_CB_1
SB_ECC_CB_2
SB_ECC_CB_3
SB_ECC_CB_4
SB_ECC_CB_5
SB_ECC_CB_6
SB_ECC_CB_7

DDR_1

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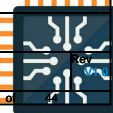
SKT_H2_CRB

DDR3 CH.B



10'06'28 ADD for TRACE Length

Desktop doesn't support ECC



CPU1I

BALLMAP_REV=1.4

A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM3
A26	VSS_003	VSS_093	AM30
A29	VSS_004	VSS_094	AM36
A35	VSS_005	VSS_095	AM37
AA33	VSS_006	VSS_096	AM38
AA34	VSS_007	VSS_097	AM39
AA35	VSS_008	VSS_098	AM4
AA36	VSS_009	VSS_099	AM40
AA37	VSS_010	VSS_100	AM5
AA38	VSS_011	VSS_101	AM10
AA6	VSS_012	VSS_102	AM11
AB5	VSS_013	VSS_103	AM14
AC1	VSS_014	VSS_104	AM17
AC6	VSS_015	VSS_105	AM19
AD33	VSS_016	VSS_106	AM22
AD36	VSS_017	VSS_107	AM24
AD38	VSS_018	VSS_108	AM27
AD39	VSS_019	VSS_109	AM30
AD40	VSS_020	VSS_110	AM31
AD5	VSS_021	VSS_111	AM32
AD8	VSS_022	VSS_112	AM33
AE3	VSS_023	VSS_113	AM34
AE33	VSS_024	VSS_114	AM35
AE36	VSS_025	VSS_115	AM36
AF1	VSS_026	VSS_116	AM5
AF34	VSS_027	VSS_117	AM6
AF36	VSS_028	VSS_118	AM7
AF37	VSS_029	VSS_119	AM8
AF40	VSS_030	VSS_120	AM9
AF5	VSS_031	VSS_121	AP1
AF6	VSS_032	VSS_122	AP11
AF7	VSS_033	VSS_123	AP14
AG36	VSS_034	VSS_124	AP17
AH2	VSS_035	VSS_125	AP22
AH3	VSS_036	VSS_126	AP25
AH33	VSS_037	VSS_127	AP27
AH36	VSS_038	VSS_128	AP30
AH37	VSS_039	VSS_129	AP36
AH38	VSS_040	VSS_130	AP4
AH39	VSS_041	VSS_131	AP40
AH40	VSS_042	VSS_132	AP5
AH5	VSS_043	VSS_133	AR11
AH8	VSS_044	VSS_134	AR14
AH12	VSS_045	VSS_135	AR17
AH15	VSS_046	VSS_136	AR18
AH18	VSS_047	VSS_137	AR19
AH21	VSS_048	VSS_138	AR27
AH25	VSS_049	VSS_139	AR30
AH27	VSS_050	VSS_140	AR36
AH36	VSS_051	VSS_141	AR5
AH37	VSS_052	VSS_142	AT1
AH38	VSS_053	VSS_143	AT10
AH39	VSS_054	VSS_144	AT12
AH40	VSS_055	VSS_145	AT13
AK1	VSS_056	VSS_146	AT15
AK10	VSS_057	VSS_147	AT16
AK13	VSS_058	VSS_148	AT17
AK14	VSS_059	VSS_149	AT2
AK16	VSS_060	VSS_150	AT25
AK22	VSS_061	VSS_151	AT27
AK28	VSS_062	VSS_152	AT28
AK31	VSS_063	VSS_153	AT29
AK32	VSS_064	VSS_154	AT3
AK33	VSS_065	VSS_155	AT30
AK34	VSS_066	VSS_156	AT31
AK35	VSS_067	VSS_157	AT32
AK36	VSS_068	VSS_158	AT33
AK37	VSS_069	VSS_159	AT34
AK4	VSS_070	VSS_160	AT35
AK40	VSS_071	VSS_161	AT36
AK5	VSS_072	VSS_162	AT37
AK6	VSS_073	VSS_163	AT38
AK7	VSS_074	VSS_164	AT39
AK8	VSS_075	VSS_165	AT4
AK9	VSS_076	VSS_166	AT40
AL11	VSS_077	VSS_167	AT5
AL14	VSS_078	VSS_168	AT6
AL17	VSS_079	VSS_169	AT7
AL19	VSS_080	VSS_170	AT8
AL24	VSS_081	VSS_171	AT9
AL27	VSS_082	VSS_172	AU1
AL30	VSS_083	VSS_173	AU15
AL36	VSS_084	VSS_174	AU26
AL5	VSS_085	VSS_175	AU34
AM1	VSS_086	VSS_176	AU4
AM11	VSS_087	VSS_177	AU6
AM14	VSS_088	VSS_178	AU8
AM17	VSS_089	VSS_179	G7
AM2	VSS_090	VSS_180	
AM21			
AM23			
AM25			
A4	VSS_NCTF_01		
AV39	VSS_NCTF_02		

9 OF 10

SKT_H2_CRB

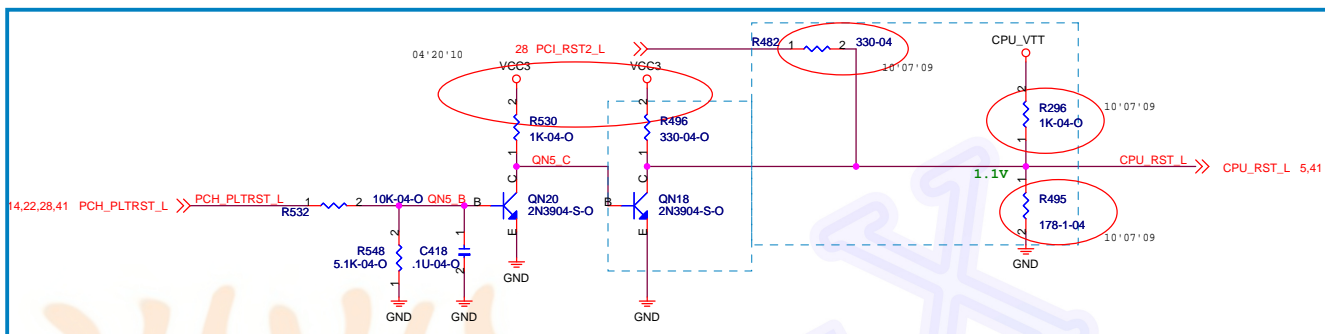
CPU1J

BALLMAP_REV=1.4

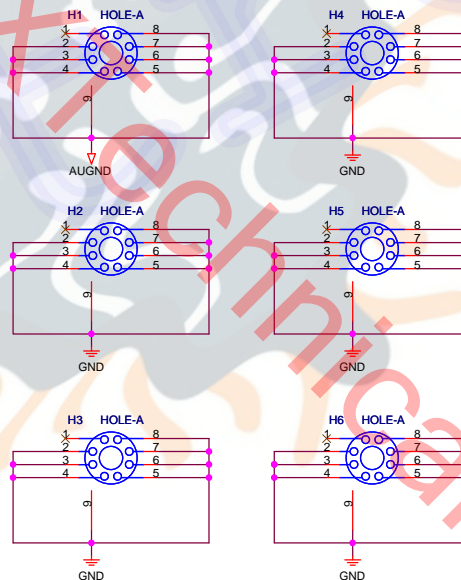
AV11	VSS_181	VSS_271	G8
AV14	VSS_182	VSS_272	H1
AV17	VSS_183	VSS_273	H17
AV3	VSS_184	VSS_274	H2
AV35	VSS_185	VSS_275	H20
AV36	VSS_186	VSS_276	H23
AV38	VSS_187	VSS_277	H26
AV39	VSS_188	VSS_278	H29
AW10	VSS_189	VSS_279	H33
AW11	VSS_190	VSS_280	H35
AW14	VSS_191	VSS_281	H37
AW16	VSS_192	VSS_282	H39
AW36	VSS_193	VSS_283	H5
AW6	VSS_194	VSS_284	H6
AY11	VSS_195	VSS_285	H9
AY14	VSS_196	VSS_286	J17
AY18	VSS_197	VSS_287	J20
AY35	VSS_198	VSS_288	J23
AY6	VSS_199	VSS_289	J26
AY8	VSS_200	VSS_290	J29
B10	VSS_201	VSS_291	J32
B13	VSS_202	VSS_292	K1
B14	VSS_203	VSS_293	K12
B17	VSS_204	VSS_294	K13
B23	VSS_205	VSS_295	K14
B26	VSS_206	VSS_296	K17
B29	VSS_207	VSS_297	K2
B32	VSS_208	VSS_298	K20
B35	VSS_209	VSS_299	K23
B38	VSS_210	VSS_300	K26
B6	VSS_211	VSS_301	K29
C11	VSS_212	VSS_302	K33
C12	VSS_213	VSS_303	K35
C17	VSS_214	VSS_304	K37
C20	VSS_215	VSS_305	K39
C23	VSS_216	VSS_306	K5
C26	VSS_217	VSS_307	K6
C29	VSS_218	VSS_308	L10
C32	VSS_219	VSS_309	L17
C35	VSS_220	VSS_310	L20
C7	VSS_221	VSS_311	L23
C8	VSS_222	VSS_312	L26
D17	VSS_223	VSS_313	L29
D2	VSS_224	VSS_314	L8
D20	VSS_225	VSS_315	M1
D23	VSS_226	VSS_316	M17
D26	VSS_227	VSS_317	M2
D29	VSS_228	VSS_318	M20
DR27	VSS_229	VSS_319	M23
D37	VSS_230	VSS_320	M26
D39	VSS_231	VSS_321	M29
D5	VSS_232	VSS_322	M33
D6	VSS_233	VSS_323	M35
D9	VSS_234	VSS_324	M37
E11	VSS_235	VSS_325	M39
E12	VSS_236	VSS_326	M5
E15	VSS_237	VSS_327	M6
E20	VSS_238	VSS_328	M9
E23	VSS_239	VSS_329	N8
E26	VSS_240	VSS_330	P1
E29	VSS_241	VSS_331	P2
E32	VSS_242	VSS_332	P36
E36	VSS_243	VSS_333	P38
E7	VSS_244	VSS_334	P40
E8	VSS_245	VSS_335	P5
F1	VSS_246	VSS_336	P6
F10	VSS_247	VSS_337	P33
F13	VSS_248	VSS_338	R37
F14	VSS_249	VSS_339	R39
F17	VSS_250	VSS_340	R8
F2	VSS_251	VSS_341	T1
F20	VSS_252	VSS_342	T5
F23	VSS_253	VSS_343	T6
F26	VSS_254	VSS_344	U8
F29	VSS_255	VSS_345	V1
F35	VSS_256	VSS_346	V2
F37	VSS_257	VSS_347	V33
F39	VSS_258	VSS_348	V34
F5	VSS_259	VSS_349	V35
F6	VSS_260	VSS_350	V36
F7	VSS_261	VSS_351	V37
F8	VSS_262	VSS_352	V38
G11	VSS_263	VSS_353	V39
G12	VSS_264	VSS_354	V40
G17	VSS_265	VSS_355	V5
G20	VSS_266	VSS_356	W6
G23	VSS_267	VSS_357	Y5
G26	VSS_268	VSS_358	Y8
G29	VSS_269	VSS_359	
G34	VSS_270	VSS_360	
G7			
AY37	VSS_NCTF_03		
B3	VSS_NCTF_04		

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SKT_H2_CRB



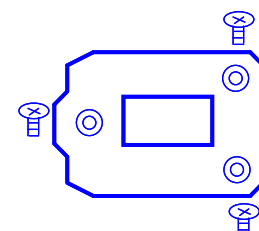
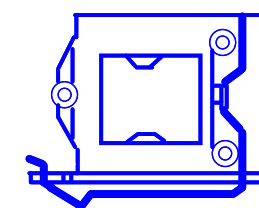
PLTRST_L Driving Circuit



11-018-115021 CPU SMD SOCKET
SOCKET.CPU..LGA 1155P SMD.BLACK.PE115527-4041-01P.
LEAD-FREE.FOXCORN

20-800-004711 CPU SOCKET STEEL
SUBASSY.STEEL.LGA 1156P.W/
BACK PLATE.PT44A11-6401.LEAD-FREE (RoHS).FOXCORN

CPU(104)
CPU_SUBASSY_STEEL



01D201-000060 PCH E80

Elitegroup Computer Systems

Title

CPU - GND, CPU_RST_L

Size

Document Number

Q67/ Q65/ H67/ H61 H2-AD

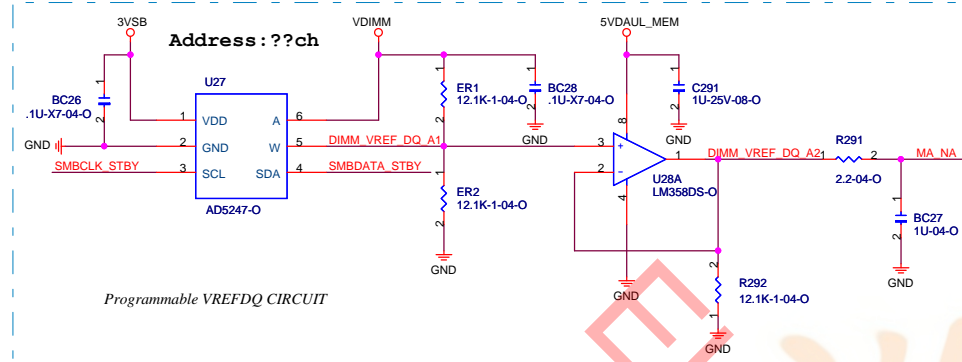
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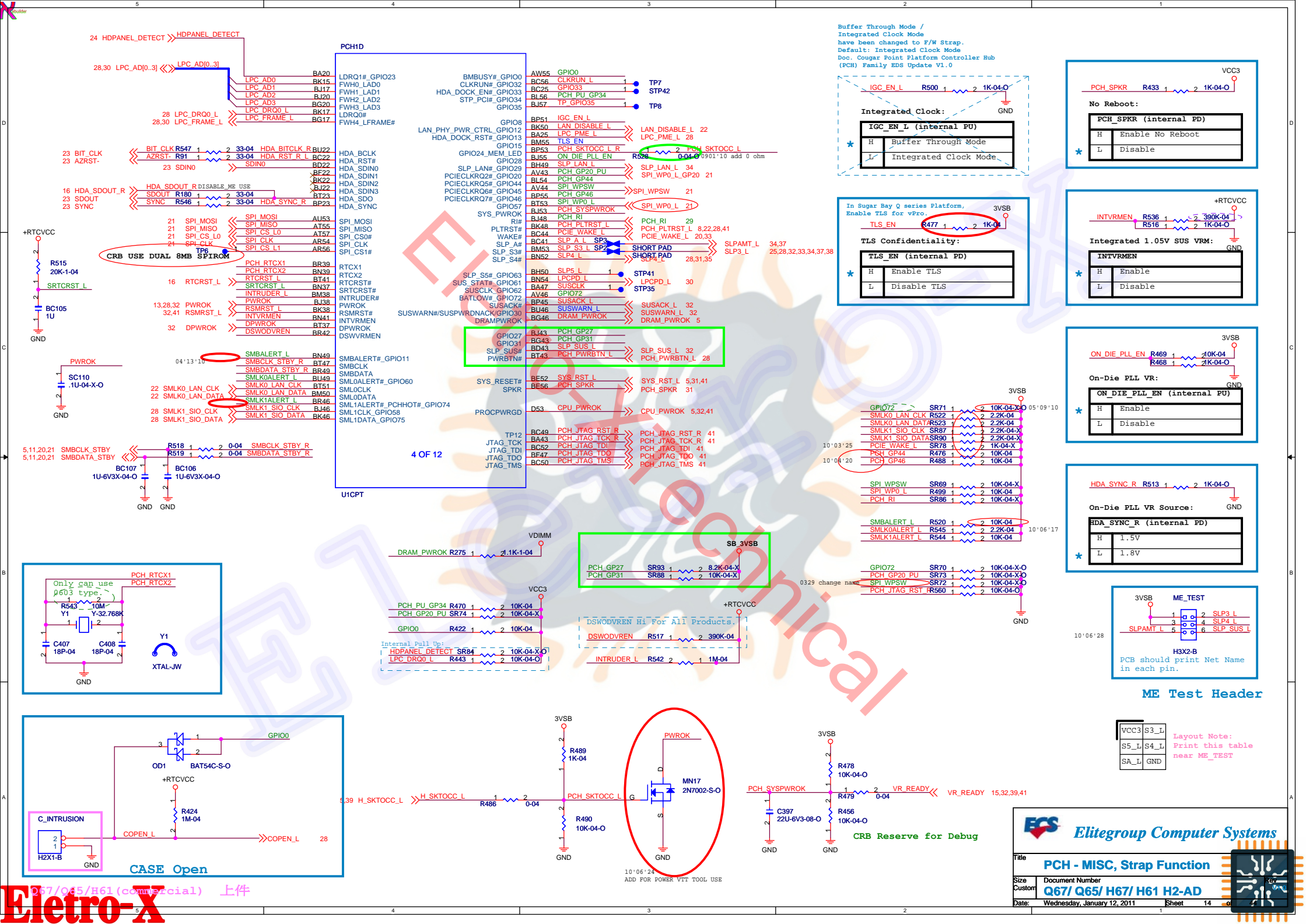
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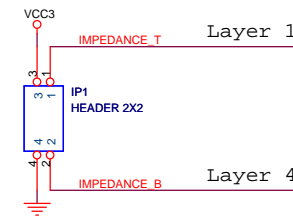
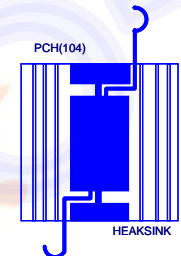
Sheet 8



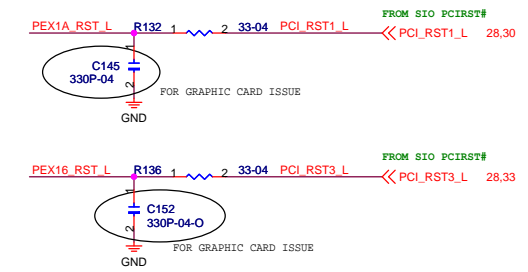
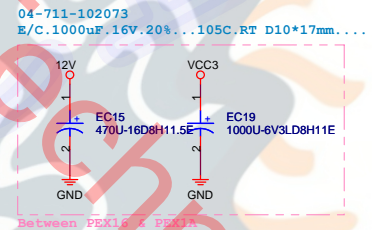
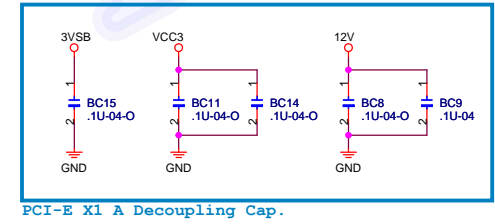
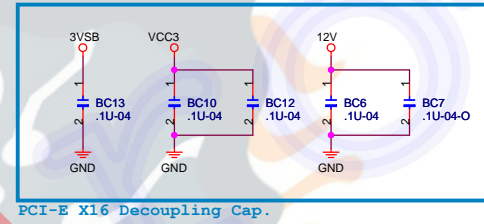
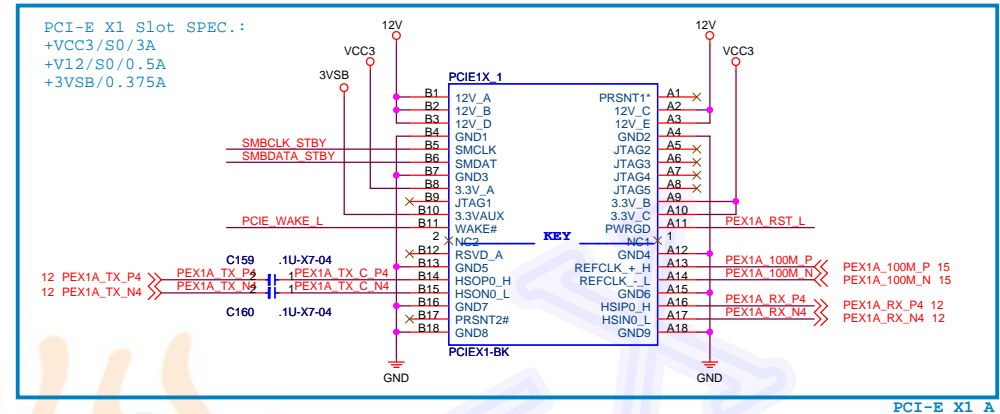
Ma

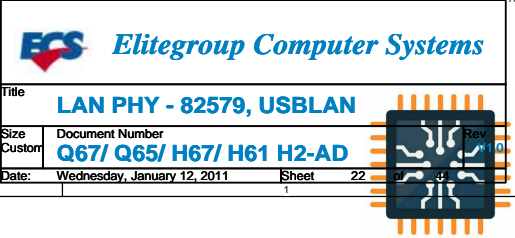




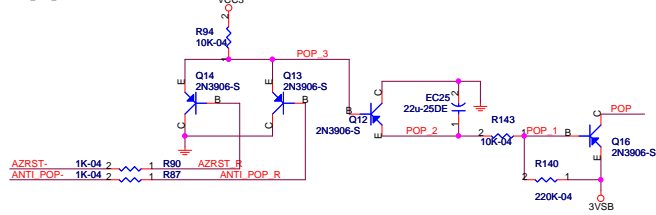


PCI-E X16 Slot SPEC.:
 +VCC3/S0/3A
 +V12/S0/5.5A
 +3VSB/0.375A

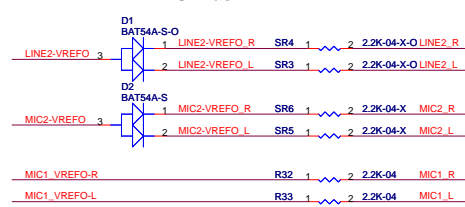




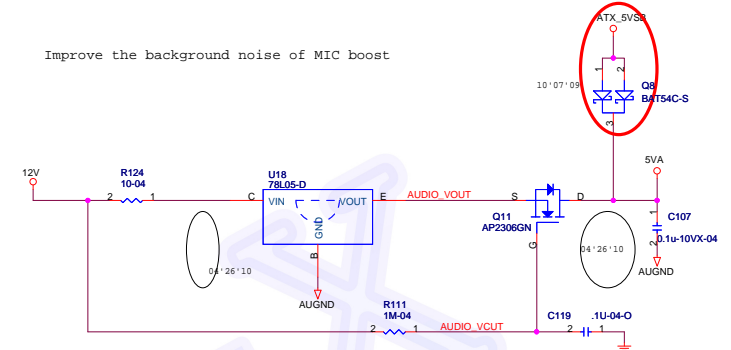
Depop schematic



MIC Bias

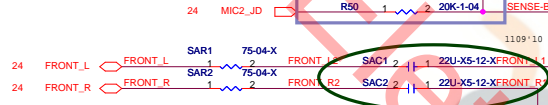


Improve the background noise of MIC boost



Place near Chip

Resistors Networks



ACODEC1

ALC662-VC-GRS

Place near Chip

Resistors Networks

Place near Chip

Resistors Networks

Place near Chip

Resistors Networks

Place near Chip

Resistors Networks

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Resistors Networks

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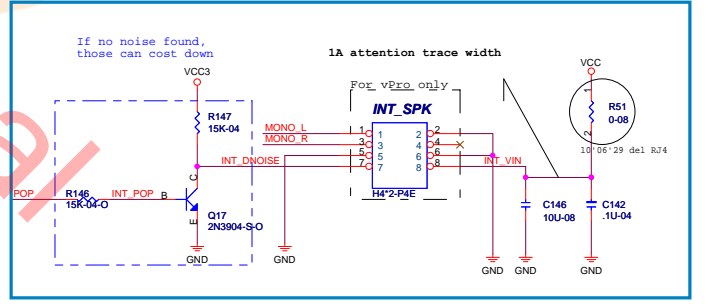
Resistors Networks

Place near Chip

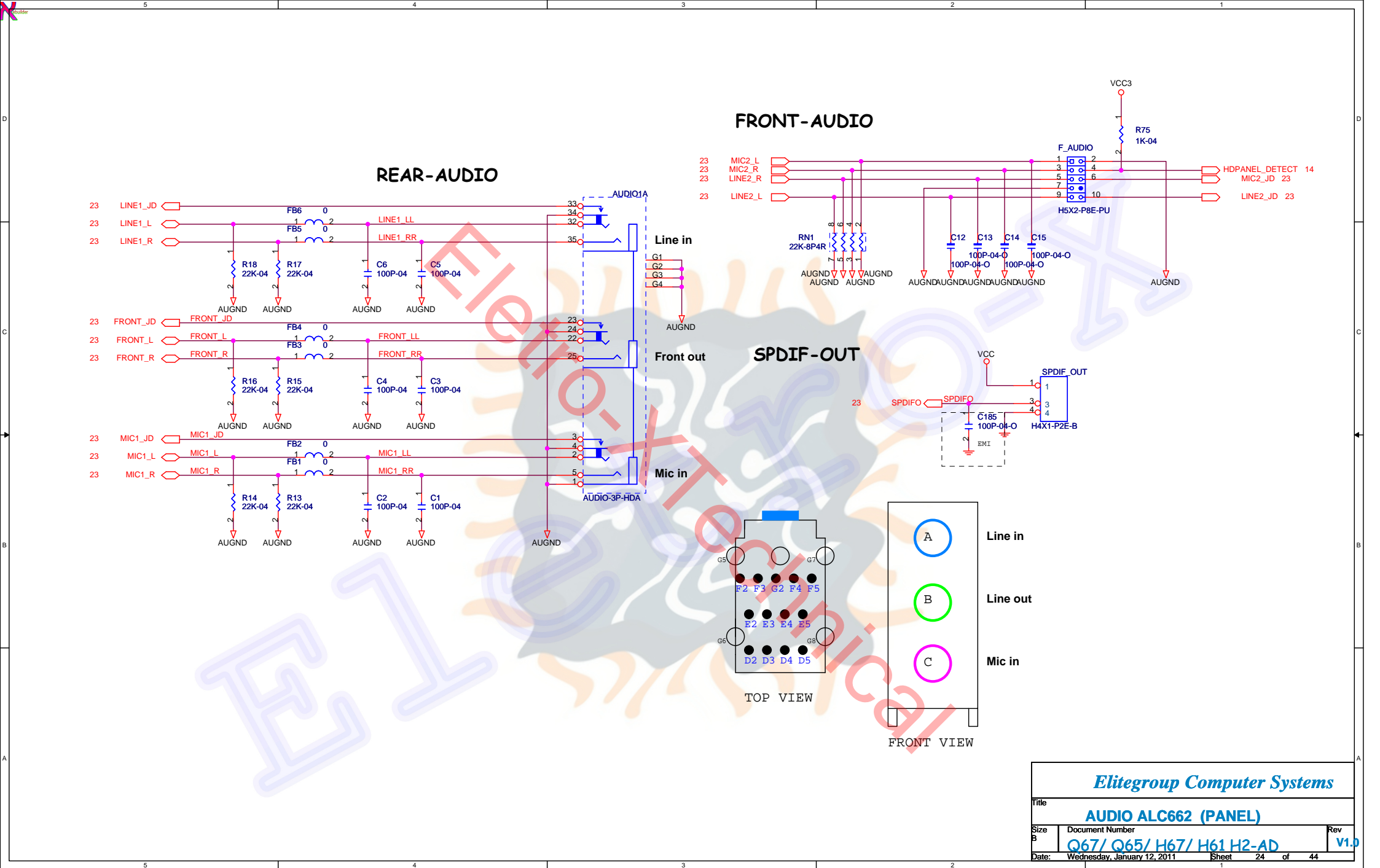
Resistors Networks

Place near Chip

Resistors Networks

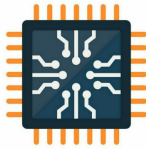


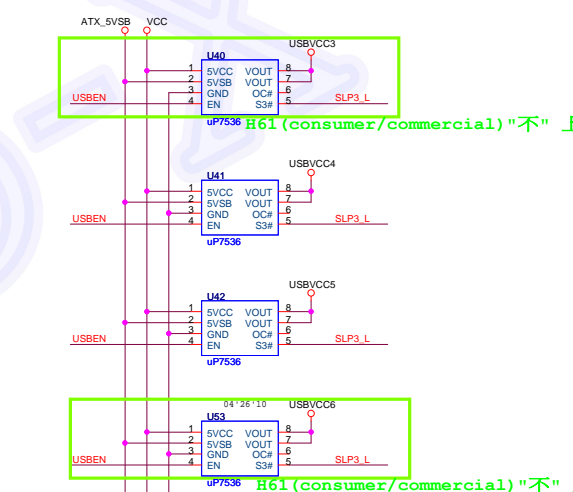
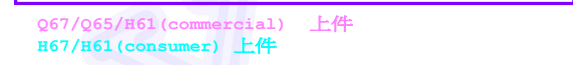
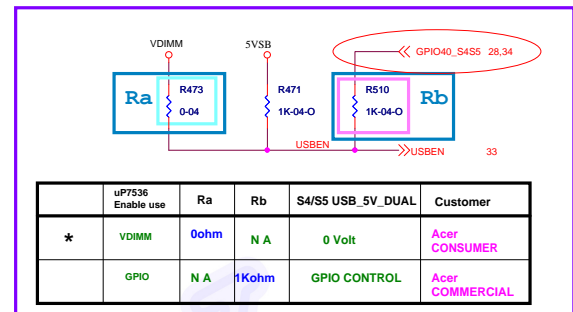
"INTERNAL SPEAKER"
FOR COMMERCIAL AND AIO SERIES USE



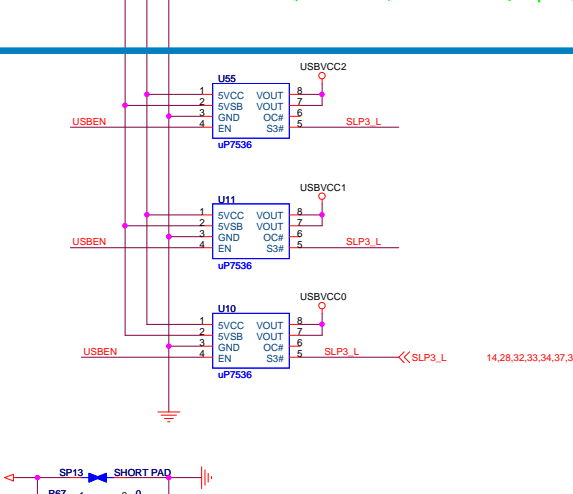
Elitegroup Computer Systems



Title			AUDIO ALC662 (PANEL)	
Size	Document Number		Rev	
B	Q67/ Q65/ H67/ H61 H2-AD		V1.0	
Date:	Wednesday, January 12, 2011		Sheet	24 of 44



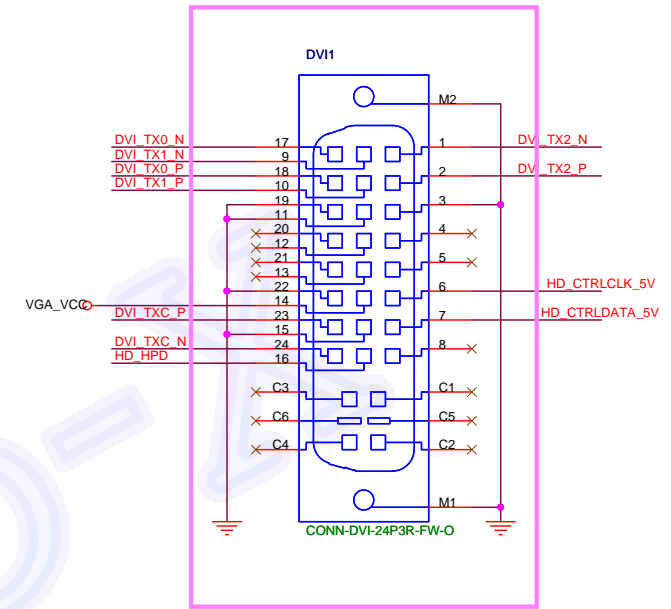


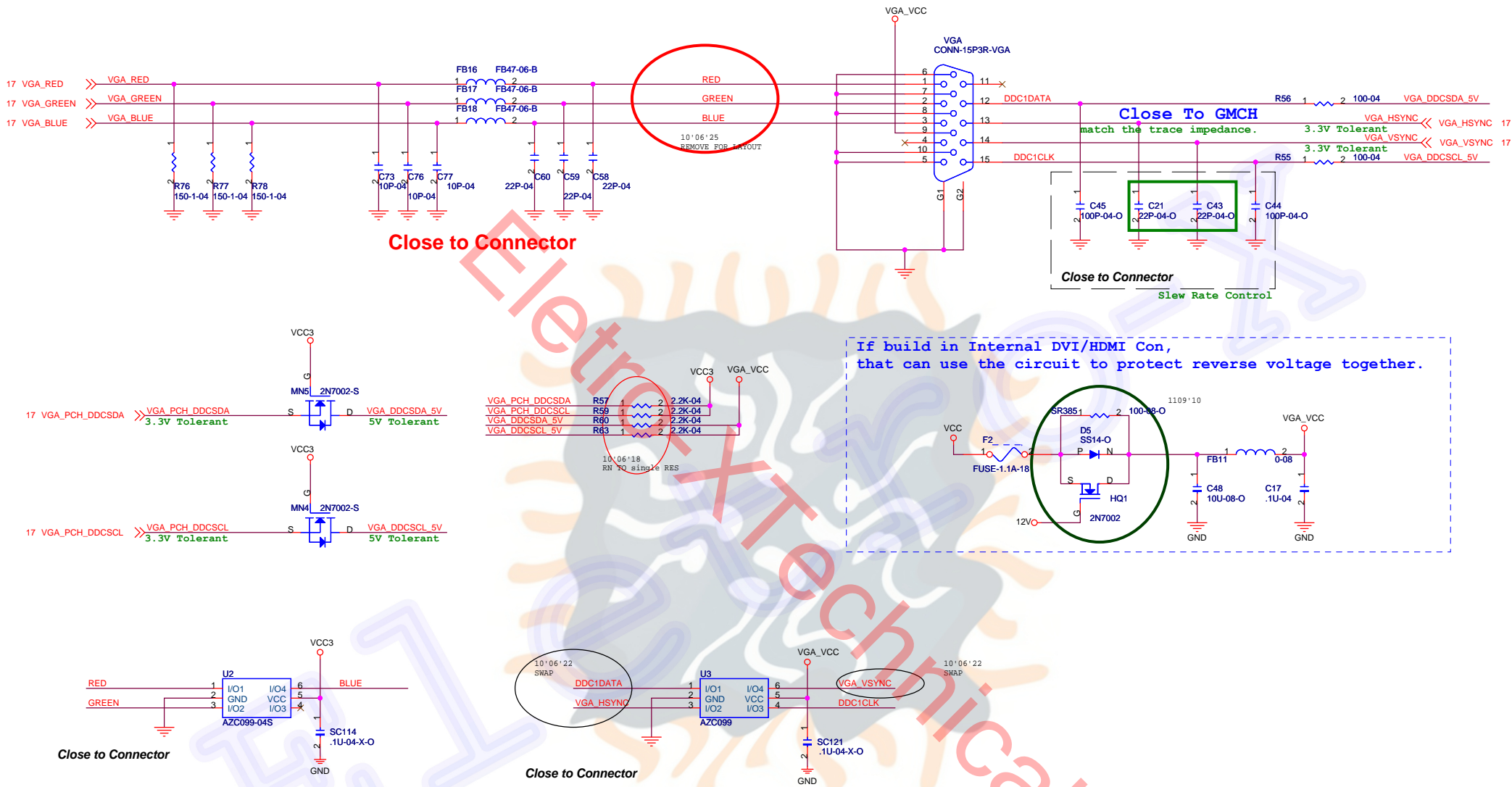
REAR PANEL USB HEADER



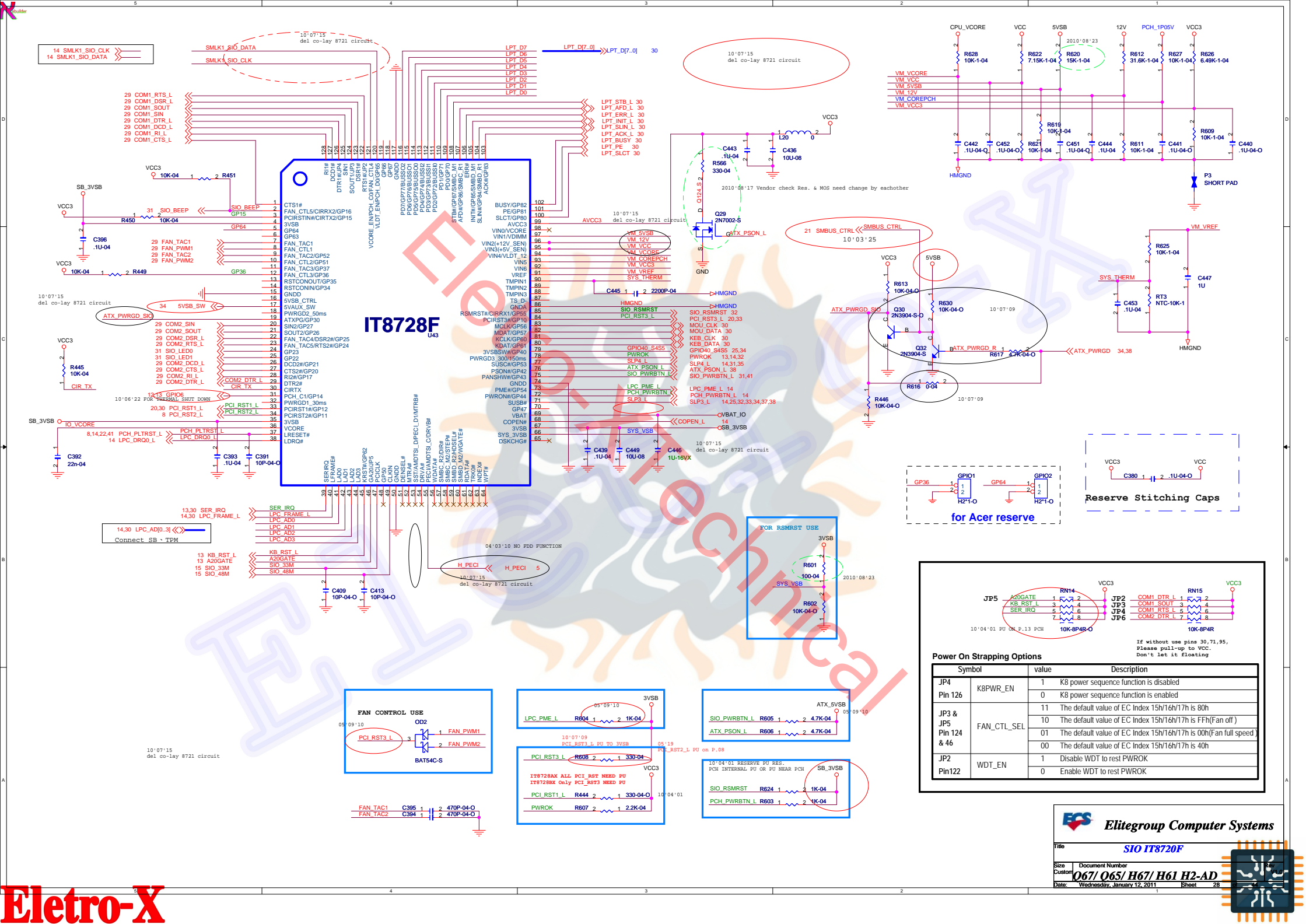
 	
Title	
USB - PWR/CONN/HDR	
Size	Document Number
Custom	Q67/ Q65/ H67/ H61 H2-AD
Date:	Wednesday, January 12, 2011 Sheet 25

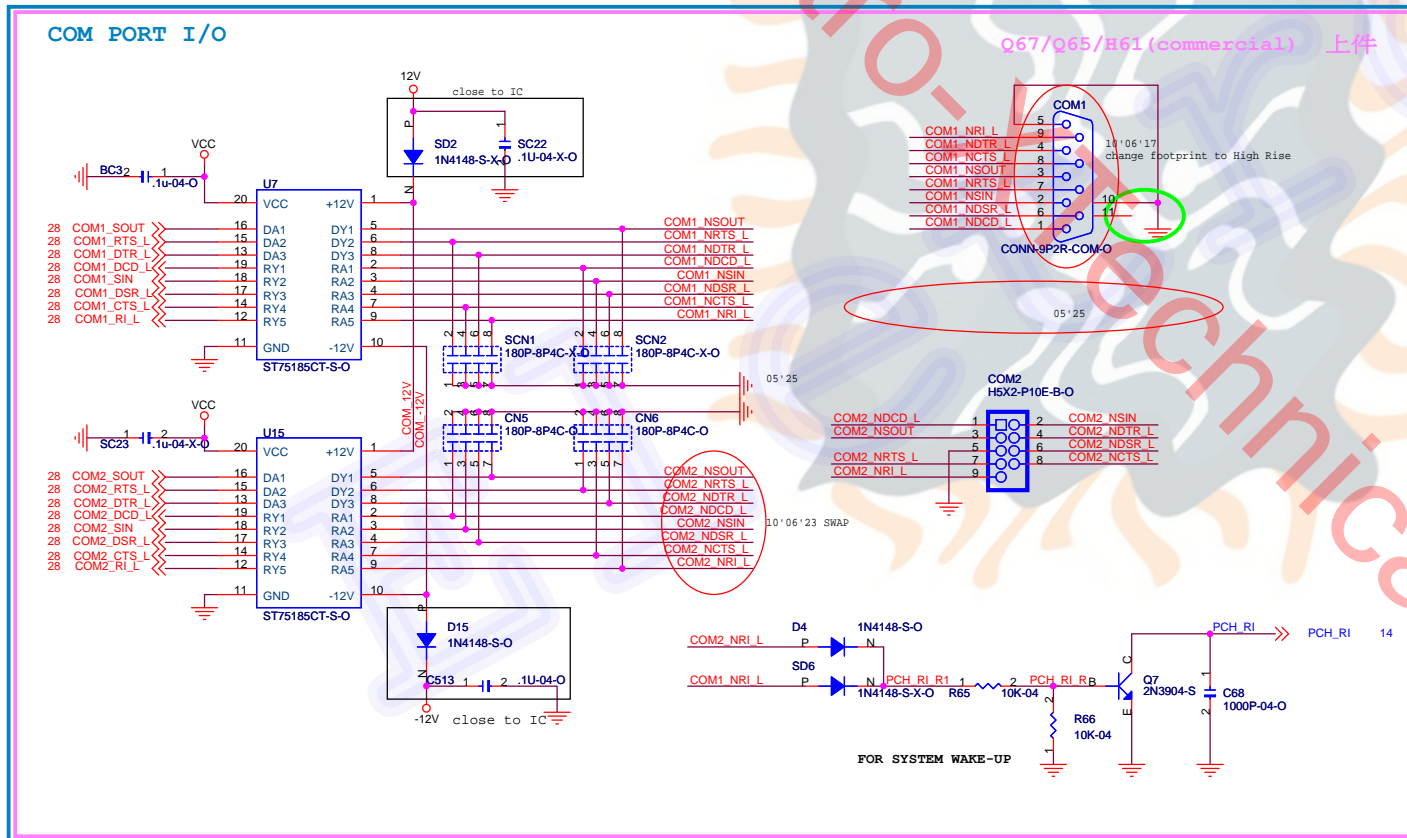
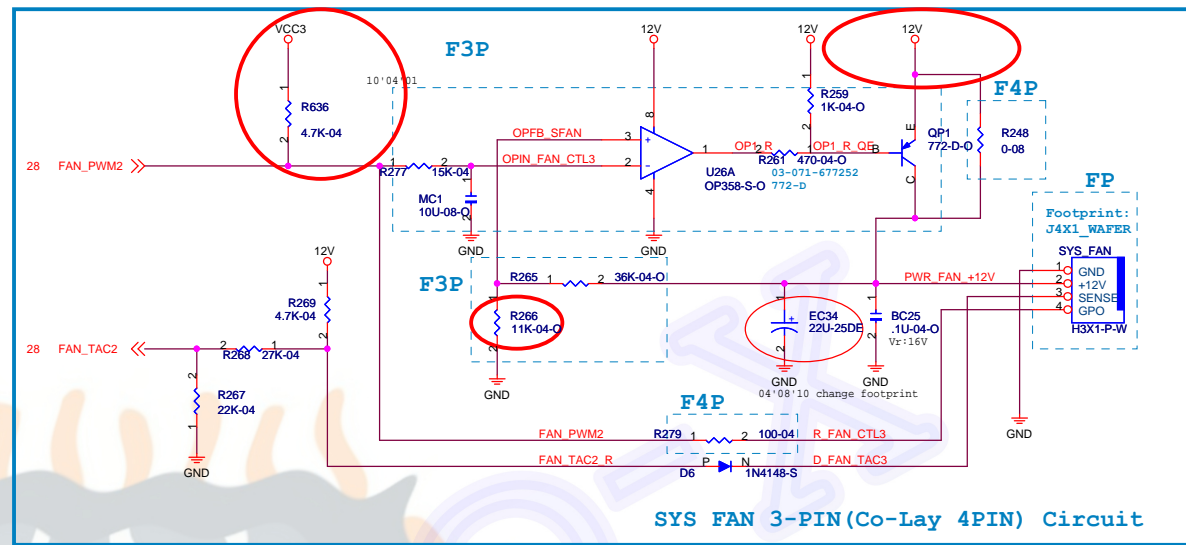
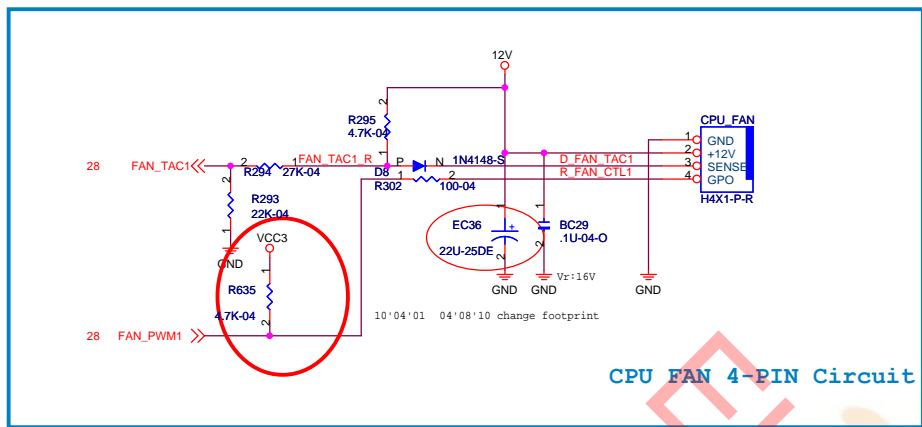
11/10





Elitegroup Computer Systems			
Title			
VGA CONNECTOR			
Size	Document Number	Rev	
Custom	Q67/ Q65/ H67/ H61 H2-AD	V1.0	
Date:	Wednesday, January 12, 2011	Sheet	27 of 27





PWR FAN:

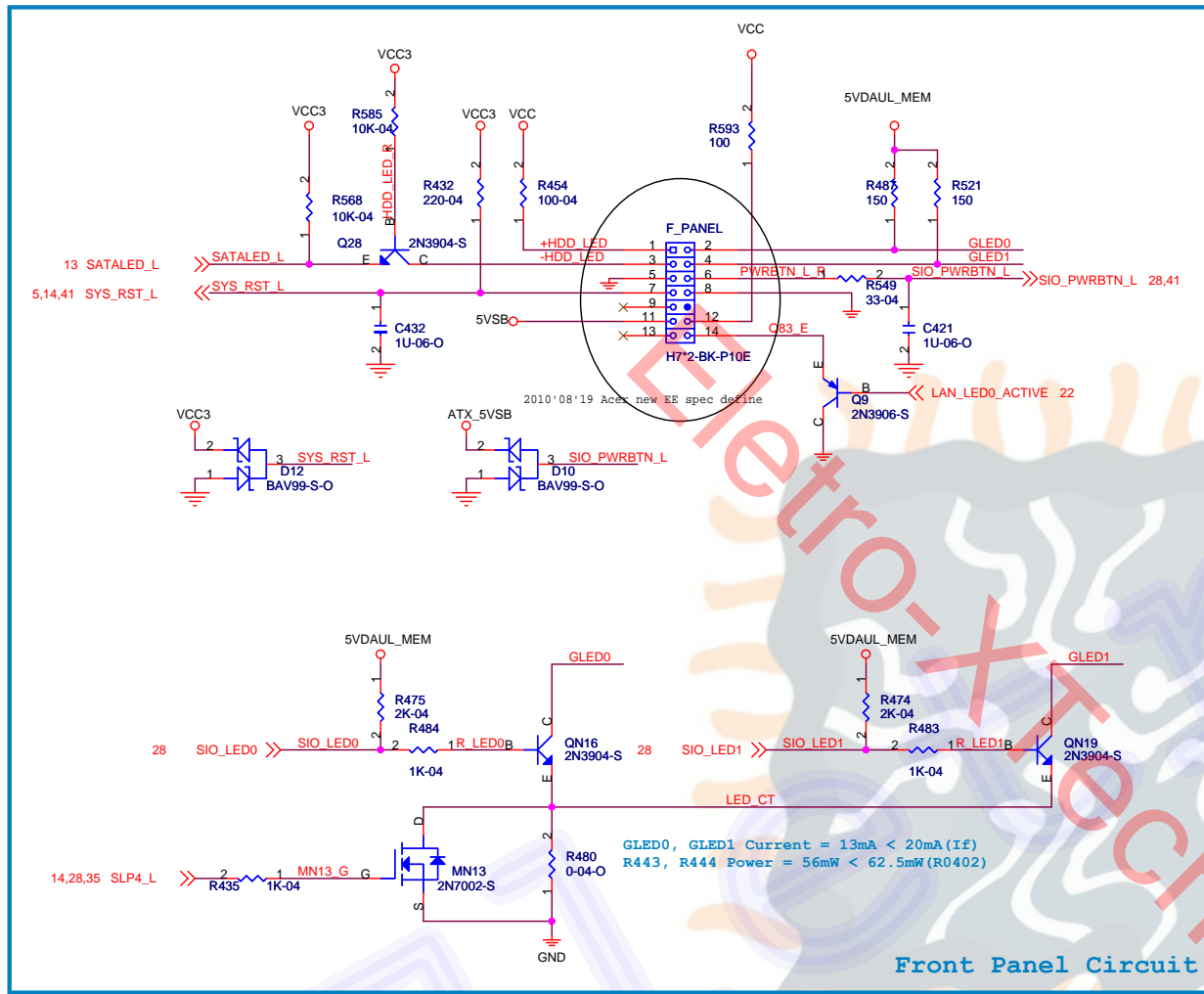
MODE	F3P	F4P	FP Value
3PIN	V	X	H3X1-P-W
4PIN	X	V	H4X1-P-W

Elitegroup Computer Systems

FAN, COM

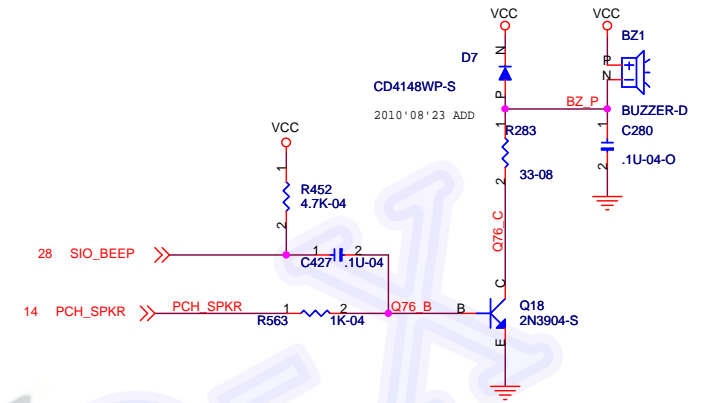
Size: Custom Document Number: **Q67/ Q65/ H67/ H61 H2-AD**

Date: Wednesday, January 12, 2011 Sheet: 29



Front Panel Circuit

Buzzer Circuit



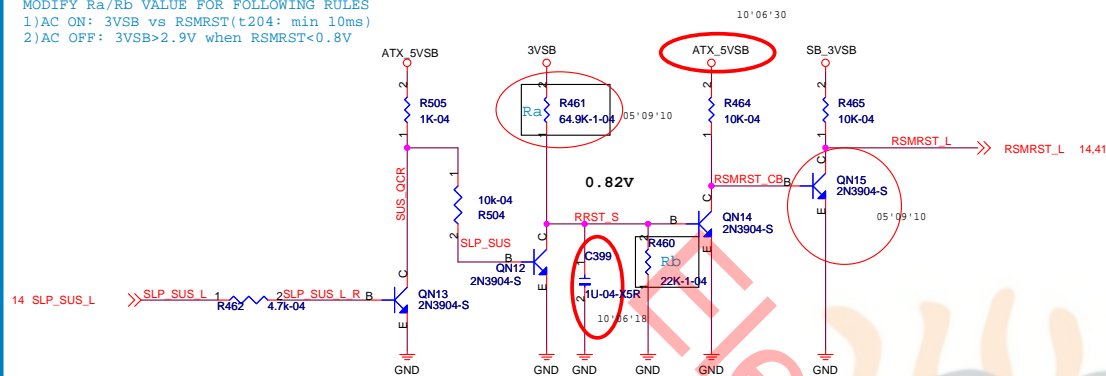
Elitegroup Computer Systems

Title			F_PANEL, BUZ
Size	Document Number	Rev	
B	Q67/ Q65/ H67/ H61 H2-AD	V1.0	
Date:	Wednesday, January 12, 2011	Sheet	31 of 44

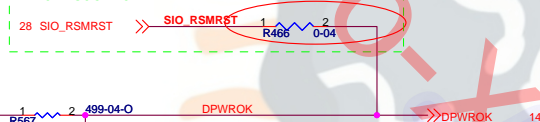


MODIFY Ra/Rb VALUE FOR FOLLOWING RULES

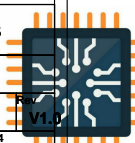
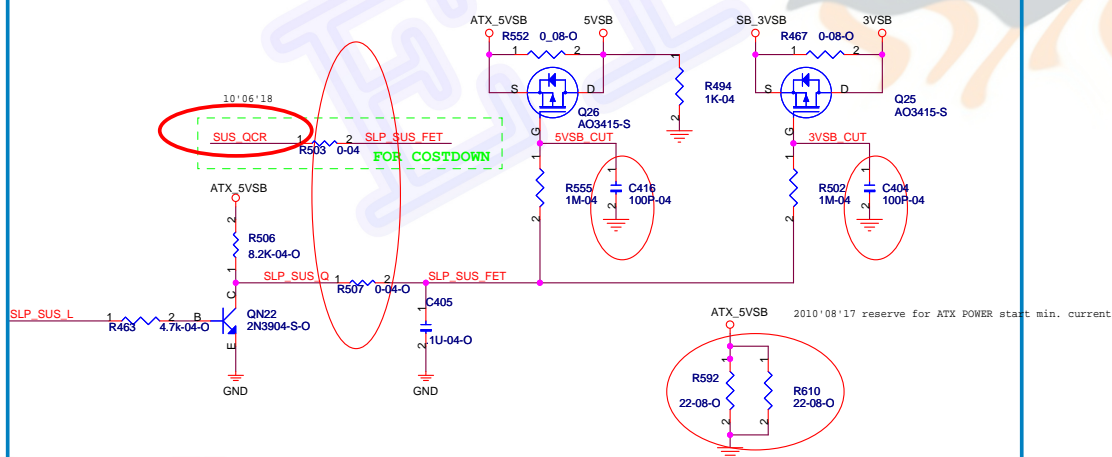
- 1) AC ON: 3VSB vs RSMRST(t204: min 10ms)
- 2) AC OFF: 3VSB>2.9V when RSMRST<0.8V

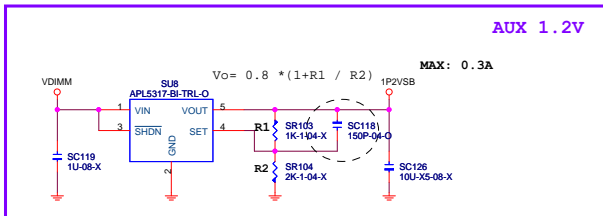
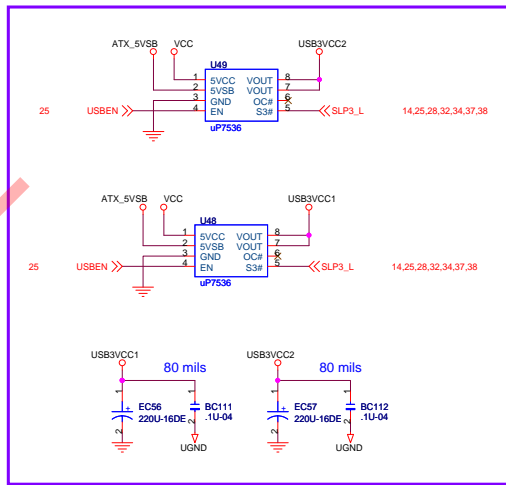
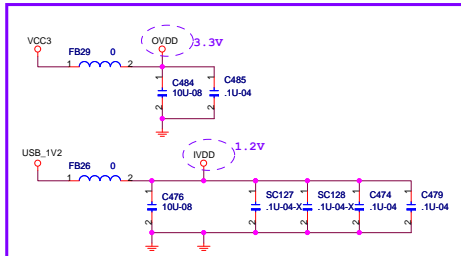
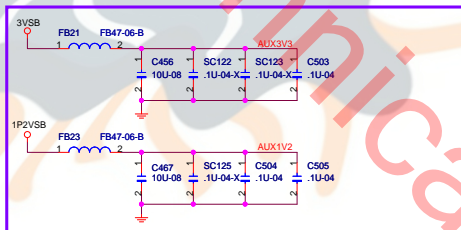
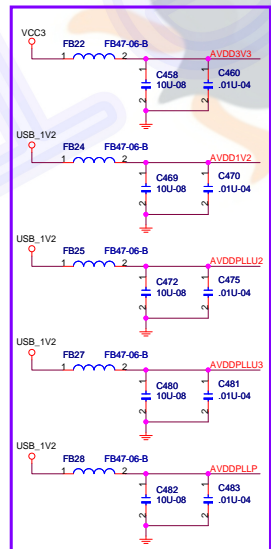
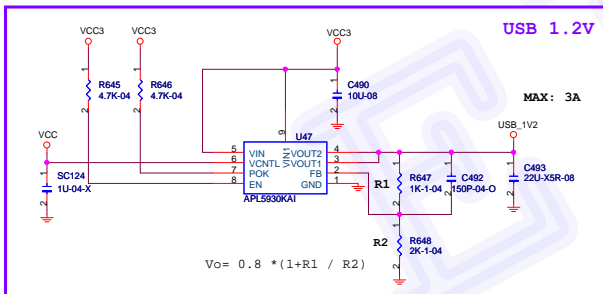
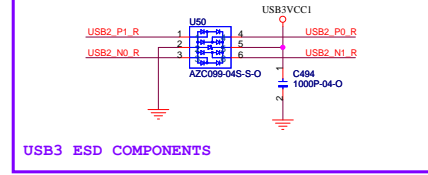
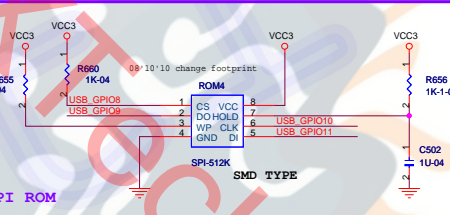
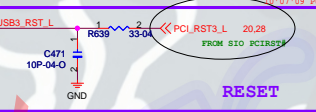
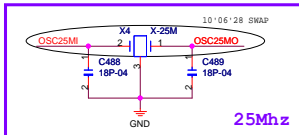
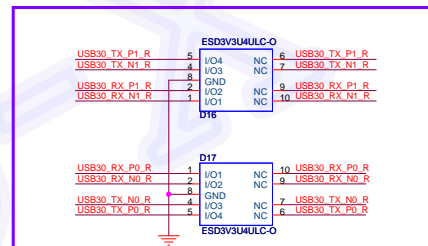
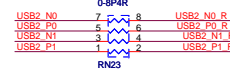
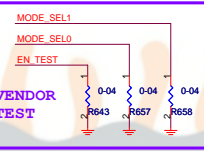
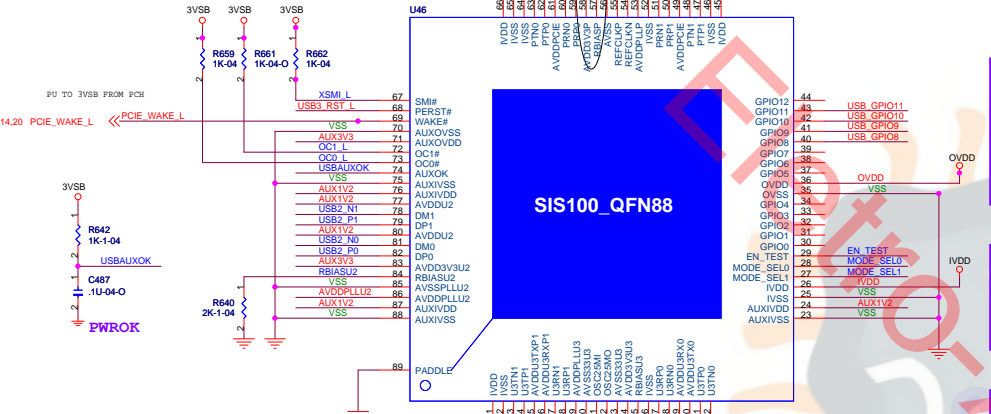
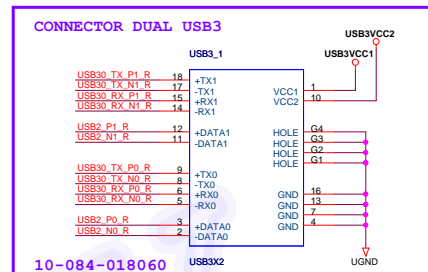
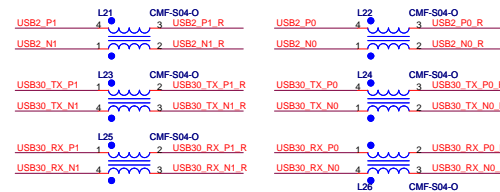
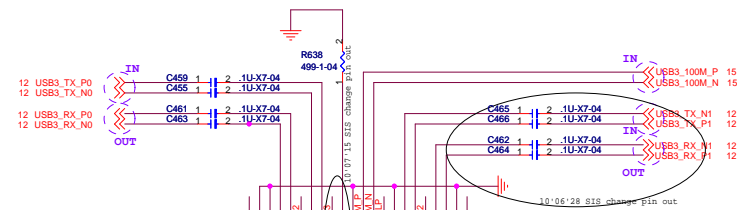


FOR COSTDOWN



SUS QCR 1 2 SLP SUS FET
R503 0-04
FOR COSTDOWN





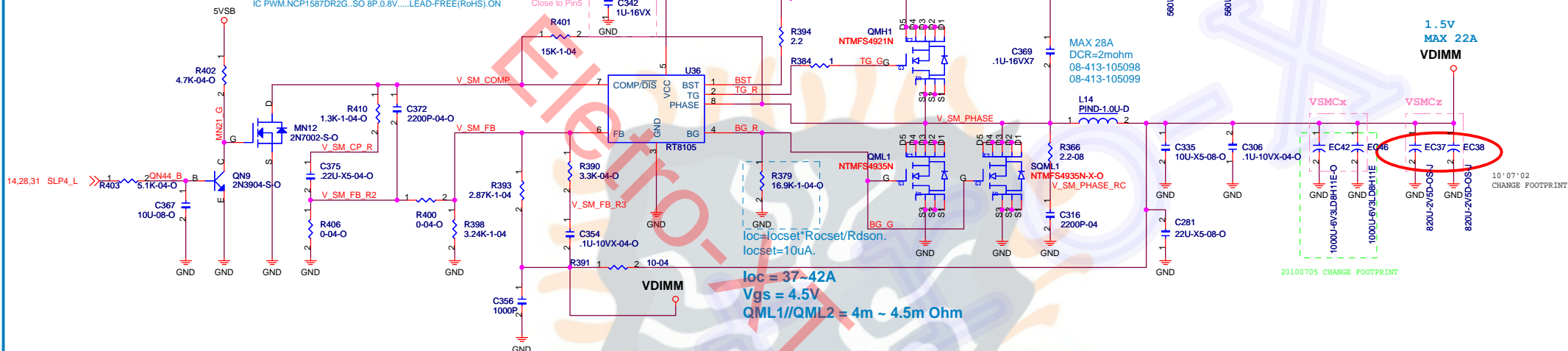
VD IMM

SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

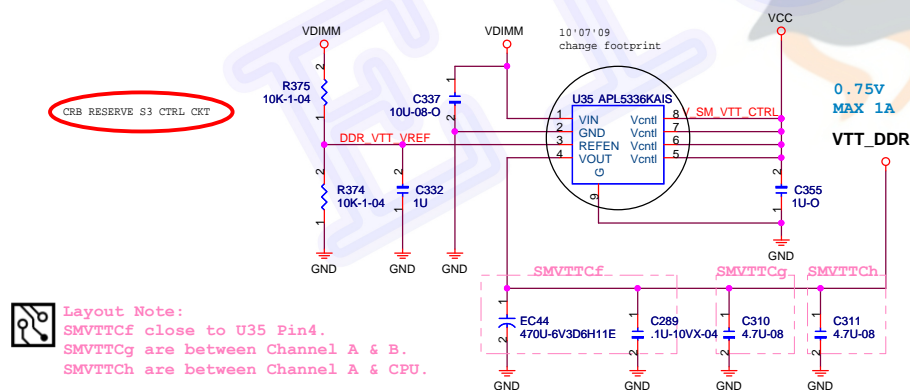
NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.

02-436-587890

IC PWM,NCP1587DR2G..SO 8P,0.8V.....LEAD-FREE(RoHS).ON



DDR VTT



Layout Note:
SMVTTc close to U35 Pin4.
SMVTTc are between Channel A & B.
SMVTTCh are between Channel A & CPU.

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



- I_{SS} is the soft-start current source at the 20 μ A limit
- V_{SRFF} is the buffered V_{RFF} reference voltage

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V _{SREF}	V _{OUT}
1	1	SW0	V _{SET1}	V _{OUT1}
1	0	SW1	V _{SET2}	V _{OUT2}
0	1	SW2	V _{SET3}	V _{OUT3}
0	0	SW3	V _{SET4}	V _{OUT4}

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad (\text{EQ. 21})$$

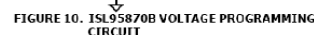
The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}} \right) \quad (\text{EQ. 22})$$

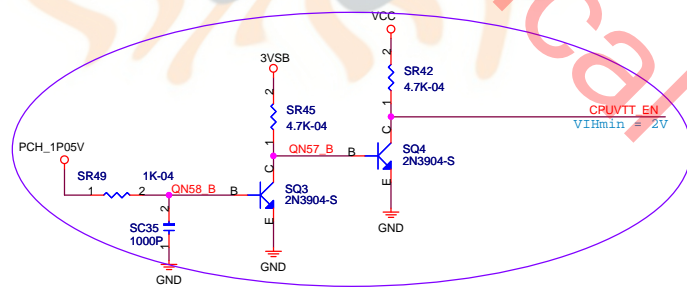
The ISL95870B V_{SET3} setpoint is written as Equation 23:

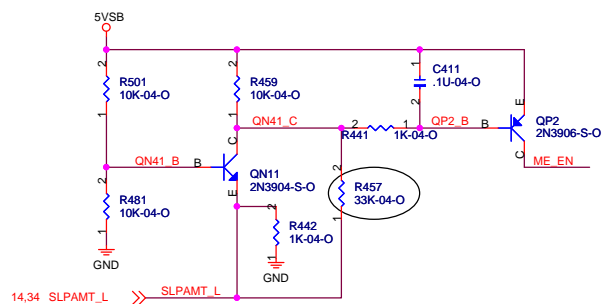
$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}} \right) \quad (\text{EQ. 23})$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

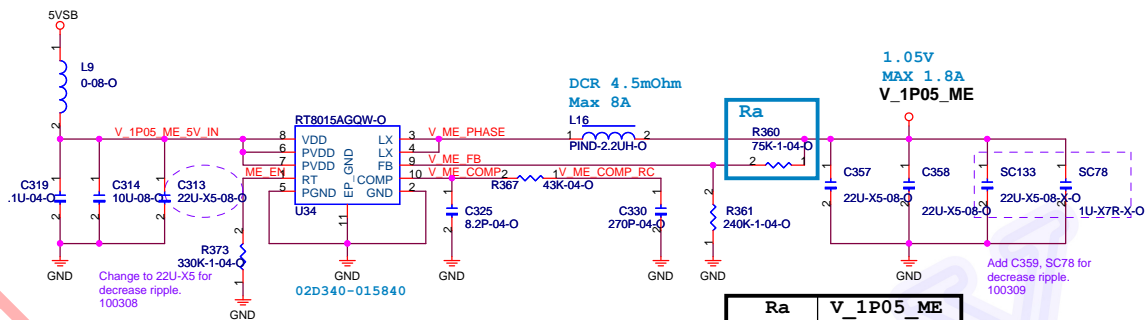
$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}} \right) \quad (\text{EQ. 24})$$


Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC





SLPAMT_L	EN	V_1P05_ME
High	5VSB	Enable
Low	0 V	Disable

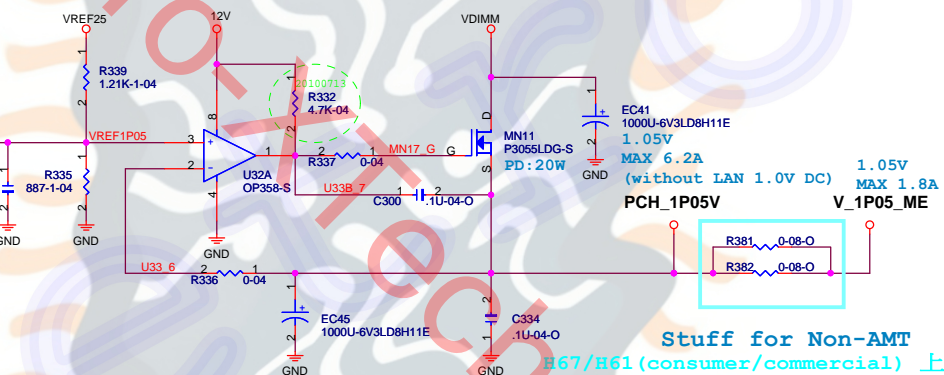
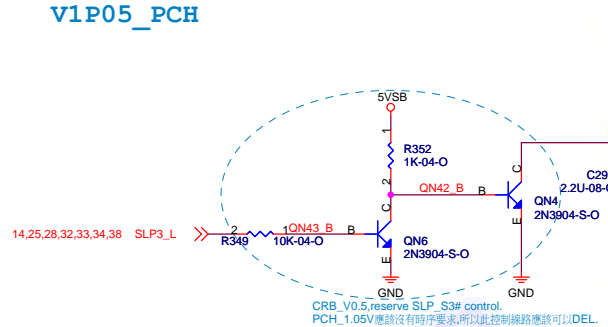


Ra	V_1P05_ME
75K	1.05V
90K	1.1V

V1P05_ME

Q67/Q65 上件

V1P05_PCH



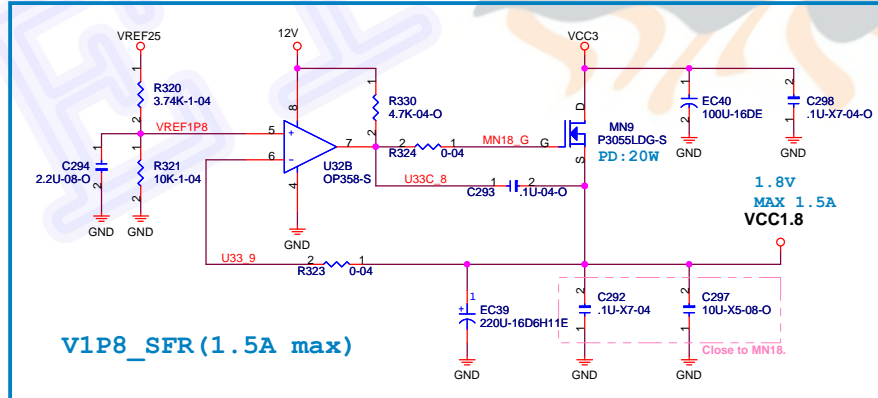
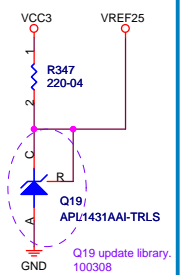
Stuff for Non-AMT

B67/H61 (consumer/commercial) 上件

BOM Note:

02-340-015840...dn10_r8106a
IC REG.RT8015AGQW.WDFN 10P.3A.LEAD-FREE(RoHS/HF).
RICHTER
08-413-225094...choke_2r2m_pt4d9x4d6mm
POWER IND.2.2uH.20%.8A.4.5m OHM.DIP 2P.8.2*8.2*7.5*6.7
mm.AKL0806MN-2R2M-L3.2....LEAD-FREE(RoHS).MAGIC
05-152-750113
RES.75K.1/16W.1%.SMD 0402....LEAD-FREE(RoHS/HF).
05-152-430103
RES.43K.1/16W.5%.SMD 0402....LEAD-FREE(RoHS/HF).
05-152-240114
RES.240K.1/16W.1%.SMD 0402....LEAD-FREE(RoHS/HF).
04-880-828100
C/C.8.2pF.50V.0.25pt..NPO...SMD 0402....LEAD-FREE(RoHS/HF).

VREF25



V1P8_SFR(1.5A max)

Elitegroup Computer Systems

Title	DC/DC V1P05_PCH,ME/V1P8_SFR
Size	Document Number
Custom	Q67/ Q65/ H67/ H61 H2-AD
Date:	Wednesday, January 12, 2011
Sheet	37

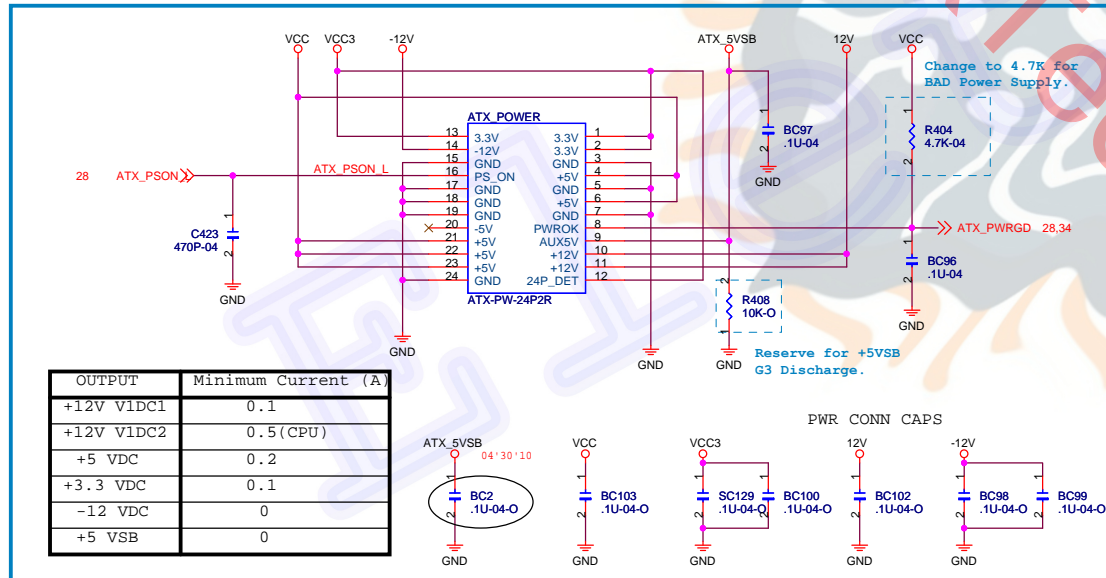
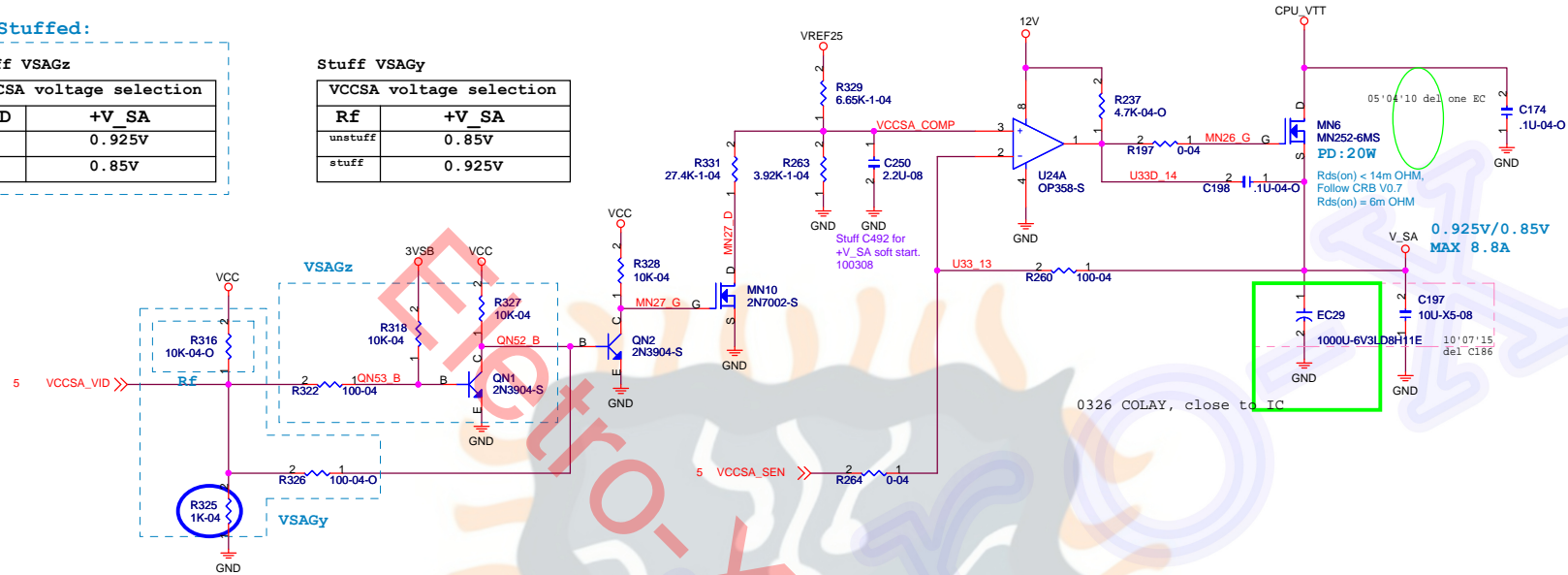
Default Stuffed:

Stuff VSAGz

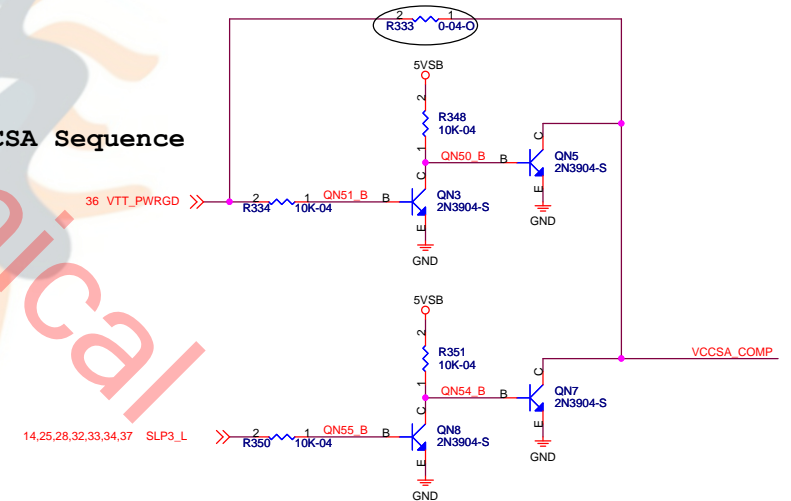
VCCSA voltage selection	
VID	+V SA
0	0.925V
1	0.85V

Stuff VSAGy

VCCSA voltage selection	
Rf	+V SA
unstuff	0.85V
stuff	0.925V



VCCSA Sequence



ATX Power 24PIN

Elitegroup Computer Systems

DC/DC VCCSA, ATXPWR

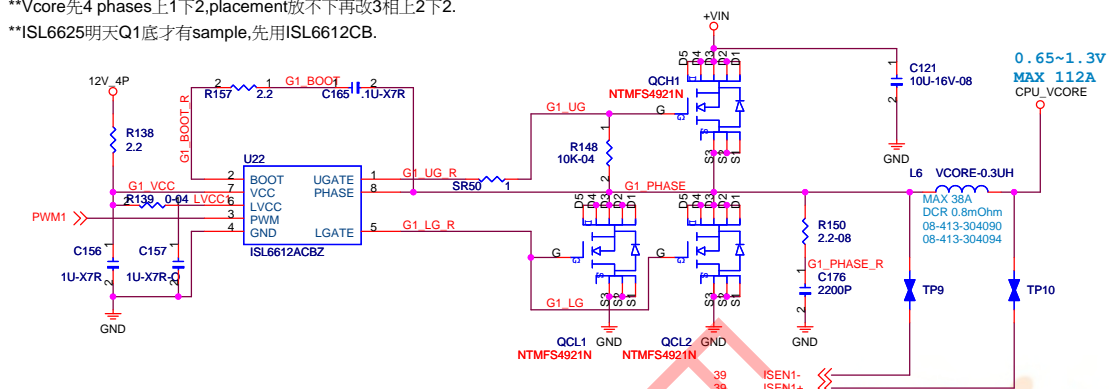
Size: Document Number
Custom: Q67/ Q65/ H67/ H61 H2-AD

Date: Wednesday, January 12, 2011 Sheet 38

**Vcore先4 phases上1下2,placement放不下再改3相上2下2.

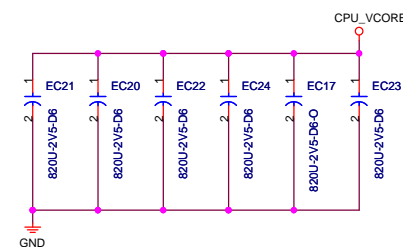
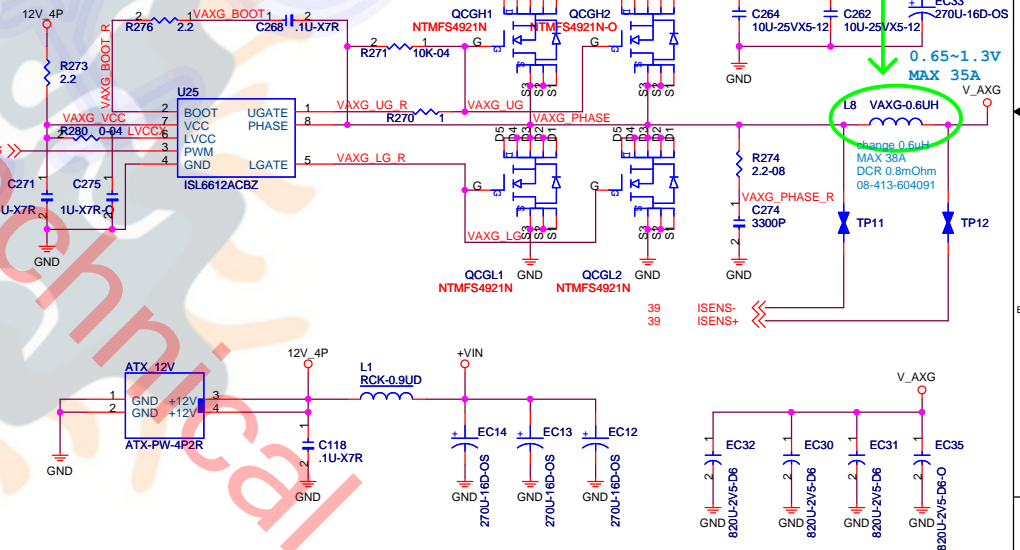
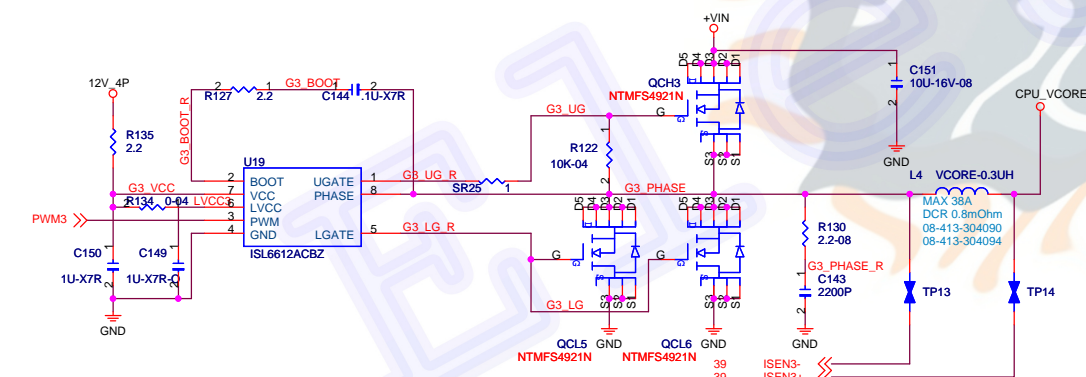
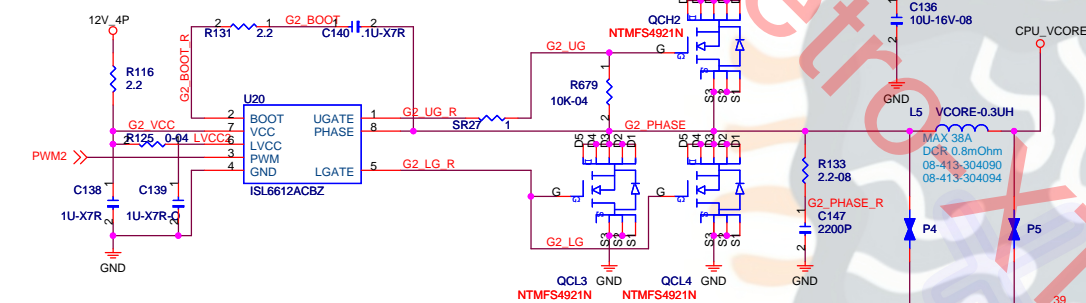
**ISL6625明天Q1底才有sample,先用ISL6612CB.

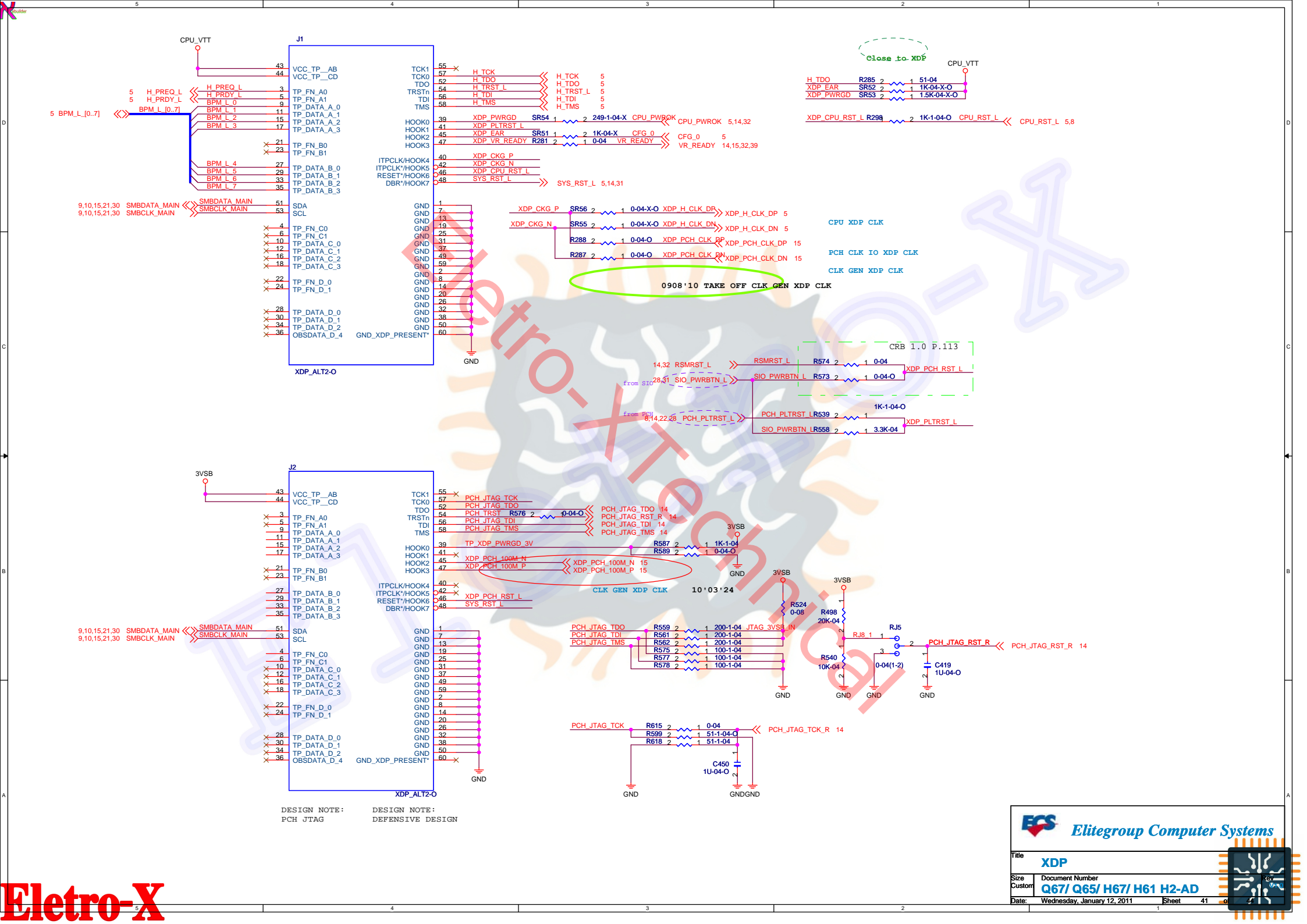
02-415-612672
IC DRIVER:ISL6612ACBZ..SO 8P,LEAD-FREE,INTERSIL



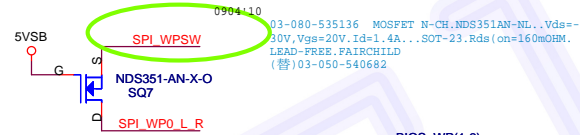
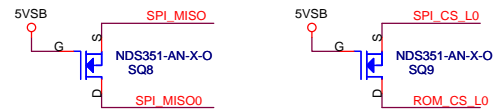
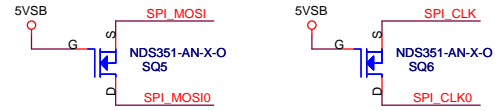
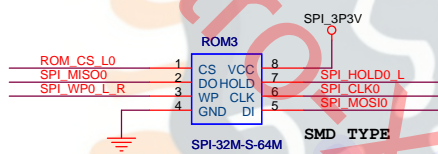
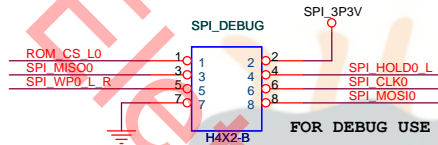
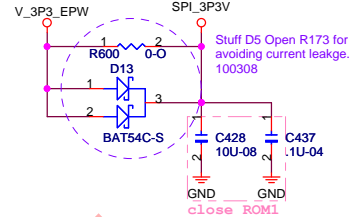
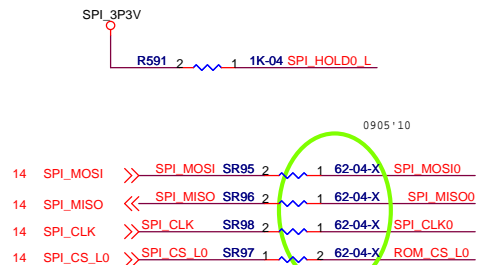
Stuff for ISL6612,
Open for ISL6625.

Open for ISL6612,
Stuff for ISL6625.





SPI ROM Circuit

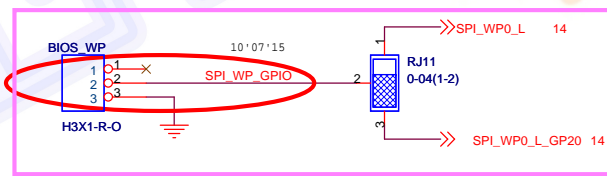


BIOS_WP(1-2)

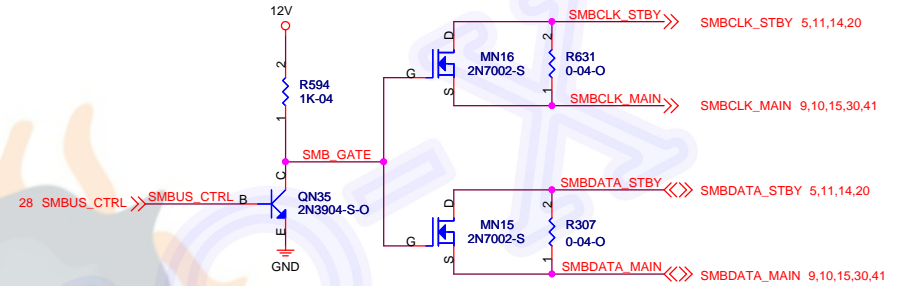
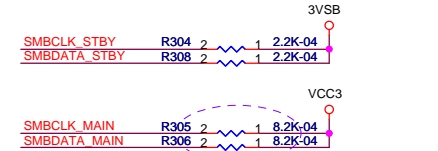


BIOS WP Jumper:

MODE	CLR_CMOS
BIOS WP	1-2
NORMAL	2-3



SMBUS Logic Circuit



Layout Note:
SMBUS Trace Max 21500MILS

PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3	LPT Detect	GPI
GPIO22	VCC3	CLR_CMOS	GPI
GPIO38	VCC3	KM Detect	GPI
GPIO39	VCC3	SENSE_Header	GPI
GPIO48	VCC3	SENSE_Header	GPI
GPIO21	VCC3	COM2 Detect	GPI
GPIO36	VCC3	TCM,TPM Detect	GPI
GPIO37	VCC3	TCM,TPM Detect	GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	